12-Bit Low Power SAR ADC

NCD98010, NCD98011

The NCD98010 (unsigned output) and the NCD98011 (signed output) ADC products provide an extremely low power solution for analog to digital conversion applications using a capacitor−based successive−approximation architecture. Optimized for low power and speed, the NCD98010/1 can achieve a sample rate of 2 MSPS while consuming less than 1 mW of power. The device also features a large input voltage range of 1.65 V to 3.3 V for various applications for both analog and digital supplies. The SPI−compatible interface provides a straight−forward data−acquisition method.

Features

- Nanowatt Power Consumption
- Fully Differential Input
- 2−MSPS Throughput
- Small Package Size
- Pre−Calibrated
- SPI Interface
- These Devices are Pb−Free, Halogen Free/BFR Free and icesces a1T4 0 TD.0042 Tc.0006 T eWearable Fitness

- Portable Medical Equipment
- Glucose Meters

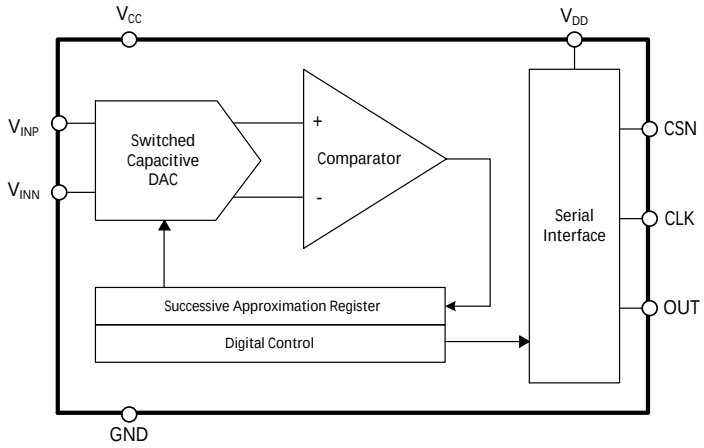
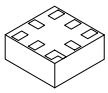


Figure 1. Block Diagram

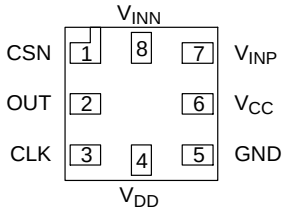


X2QFN8
DP SUFFIX
CASE 722AM

MARKING DIAGRAMS

XX = Specific Device Code
M = Date Code

PIN CONFIGURATION



X2QFN8 (Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCD98010XMXTAG	X2QFN	5000 / Tape & Reel
NCD98011XMXTAG		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PIN DESCRIPTION

X2QFN Pin No.	Name	Function
1	CSN	Chip select (active low)
2	OUT	Data Output (serialized)
3	CLK	Clock
4	VDD	Digital I/O supply voltage
5	GND	Common ground for all pins
6	VCC	Analog supply and ADC reference voltage
7	V_{INP}	Analog input, positive signal
8	V_{INN}	Analog input, negative signal

MAXIMUM RATINGS

Rating	Symbol

ELECTRICAL CHARACTERISTICS (T_J = 25°C, V_{CC} = 3 V, unless otherwise noted)

Parameter	Conditions	Symbol	Min	Ty
POWER SUPPLY REQUIREMENTS				
Analog Supply and ADC reference		V_{CC}	1.65	
Digital I/O Supply		V_{DD}	1.65	
Analog Supply Current	2 MSPS for V_{CC} = 3.6 V	I_{VCC}		
	1 MSPS for V_{CC} = 3 V			
	100 kSPS for V_{CC} = 3.6 V			
	1 MSPS for V_{CC} = 1.8 V			
Analog Power Dissipation	2 MSPS for V_{CC} = 3.6 V	P_{VCC}		
	1 MSPS for V_{CC} = 3 V			
	100 kSPS for V_{CC} = 3.6 V			
	1 MSPS for V_{CC} = 1.8 V			
Digital Supply Current Dependent on SDO loading (tested with ~7 pF)	2 MSPS for V_{DD} = 3.6 V	I_{VDD}		
	1 MSPS for V_{DD} = 3 V			
	100 kSPS for V_{DD} = 3.6 V			
	1 MSPS for V_{DD} = 1.8 V			
Standby current (CSN high) (Note 2)	V_{CC} = 3.6 V	I_{STM}		

ELECTRICAL CHARACTERISTICS (T_J = 25°C, V_{CC} = 3 V, unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS						
Total−Harmonic Distortion	f_{IN} = 1 kHz V_{CC} = 3.3 V	THD		−80		dB
	f_{IN} = 1 kHz V_{CC} = 1.8 V			−80		
Signal−to−Noise and Distortion (Note 4)	f_{IN} = 1 kHz V_{CC} = 3.3 V	SINAD	68	69		dB
	f_{IN} = 1 kHz V_{CC} = 1.8 V			62		
Spurious−Free Dynamic Range (Note 4)	f_{IN} = 1 kHz V_{CC} = 3.3 V	SFDR	69	80		dB
	f_{IN} = 1 kHz V_{CC} = 1.8 V			74		
DIGITAL INPUT/OUTPUT						
High−Level Input Voltage		V_{IH}	V_{DD}*0.7			V
Low−Level Input Voltage		V_{IL}			V_{DD}*0.3	V
High−Level Output Voltage	2 mA drive	V_{OH}	V_{DD} − 0.5 V			V
Low−Level Output Voltage	2 mA drive	V_{OL}			GND+0.5	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Standby current includes both digital and analog currents.
3. INL and DNL parameters were verified via bench testing and are not used for production screening.
4. SINAD and SFDR are tested at production and guaranteed by correlation to bench test results.

TIMING CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
TIMING SPECIFICATIONS						
Throughput		$f_{THROUGH}$			2	MSPS
Cycle Time		f_{CYCLE}	0.5			μs
Conversion Time		f_{CONV}	437.5			ns
Data Delay				1		cycle
TIMING REQUIREMENTS						
Acquisition Time (CSN high)		t_{ACQ}	62.5			ns
CLK Frequency		f_{CLK}			32	MHz
CLK Period		t_{CLK}			31.25	ns
CSN Falling to 1st SCLK falling edge		t_{CSN_SCLK}	15.75			ns
Last SCLK falling edge to CSN rising		t_{SCLK_CSN}	15.75			ns
Falling SCLK to SDO valid (Note 5)	Assumed 10 pF Load	t_{SDO_VALID}			30	ns

5. When SCLK is running at higher frequencies, the t_{SDO_VALID} of 30 ns requires SDO to be sampled on the falling edge of SCLK at the end of the bit width just before SDO changes to the next output. This will ensure acquisition of the correct data. For example, location A shown below would be the best place to sample SDO for the acquisition of bit 9.

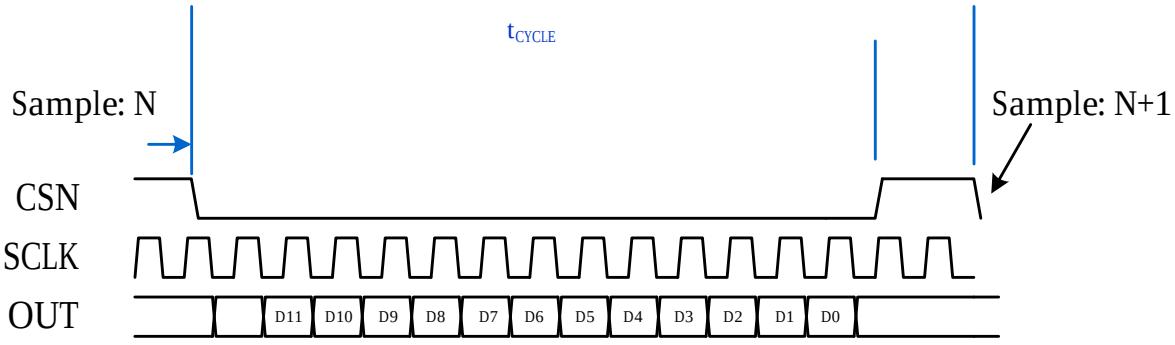


Figure 2. Serial Interface Timing

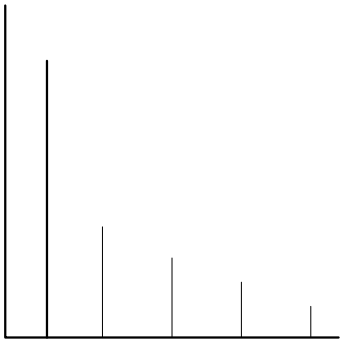


Figure 16. Spurious Free Dynamic Range in the Frequency Domain

1 μF. All decoupling capacitors must connect directly to a low impedance ground plane in order to be effective. Short traces or vias are required to minimize additional series inductance. Ceramic capacitors are recommended based on their low ESR and ESL. X7R ceramic capacitors are recommended for applications involving a wide temperature range.

Minimal Component Realization

For applications where minimizing board space trumps ADC performance, the NCD98010/1 connection diagram can be reduced as shown in Figure 21 below. The removal of the input buffering may be an option depending on the nature of the differential analog input source. Removing the anti−aliasing filter would come at the expense of reduced ENOB due to the digitization of aliased signals.

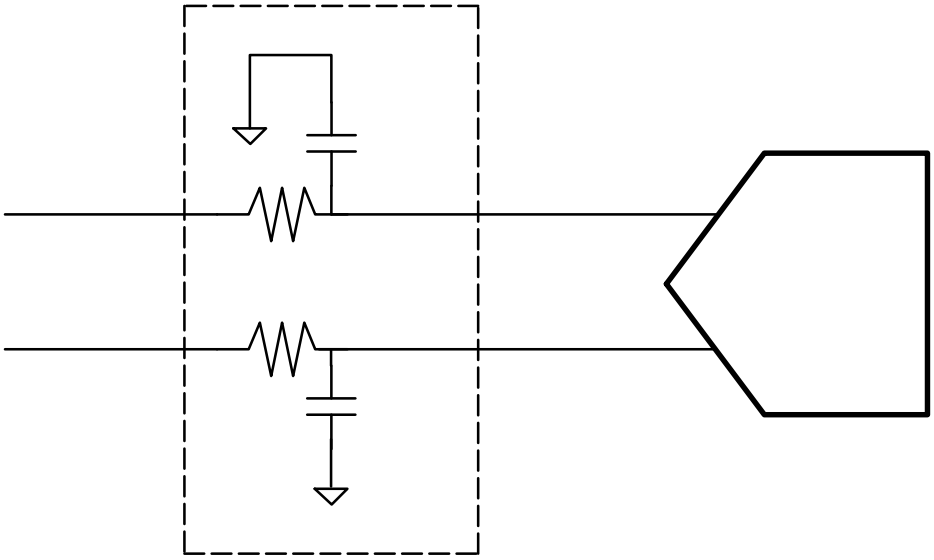
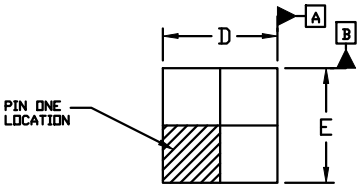


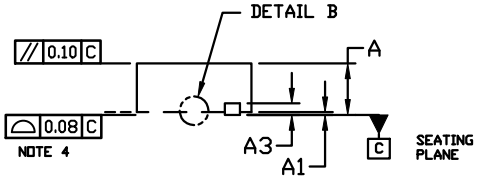
Figure 21. Reduced Component Connection Diagram

X2QFN8, 1.5x1.5, 0.5P
CASE 722AM
ISSUE O

DATE 20 JUL 2018



TOP VIEW

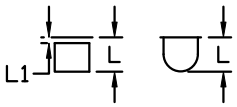


SIDE VIEW

ASME Y14.5M, 1994.

IINALS AND IS

3. DIMENSION b APPLIES TO THE PLATED TERM MEASURED BETWEEN 0.15 AND 0.20 FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



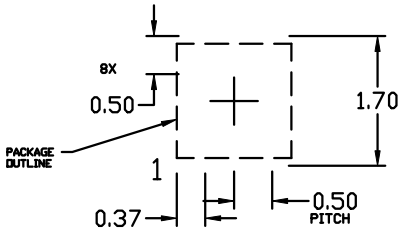
DETAIL A
ALTERNATE CONSTRUCTIONS

			MAX.
			0.40
			0.05
			0.25
D		1.50	1.55
	1.45	1.50	1.5
L		0.30	0.35
L1	-		0.10

7X

DETAIL B

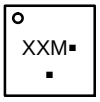
TRUCTIONS



RECOMMENDED MOUNTING FOOTPRINT

BOTTOM VIEW

GENERIC MARKING DIAGRAM*



X = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.