



3.3 V/5 V Programmable PLL Synthesized Clock Generator

50 MHz to 800 MHz

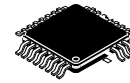
NBC12430, NBC12430A

The NBC12430 and NBC12430A are general purpose, PLL based synthesized clock sources. The VCO will operate over a frequency range of 400 MHz to 800 MHz. The VCO frequency is sent to the N-output divider, where it can be configured to provide division ratios of 1, 2, 4, or 8. The VCO and output frequency can be programmed using the parallel or serial interfaces to the configuration logic. Output frequency steps of 250 kHz, 500 kHz, 1.0 MHz, 2.0 MHz can be achieved using a 16 MHz crystal, depending on the output dividers settings. The PLL loop filter is fully integrated and does not require any external components.

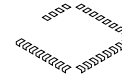
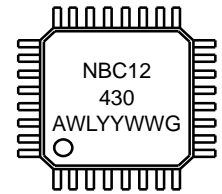
Features

- Best-in-Class Output Jitter Performance, ± 20 ps Peak-to-Peak
- 50 MHz to 800 MHz Programmable Differential PECL Outputs
- Fully Integrated Phase-Lock-Loop with Internal Loop Filter
- Parallel Interface for Programming Counter and Output Dividers During Powerup
- Minimal Frequency Overshoot
- Serial 3-Wire Programming Interface
- Crystal Oscillator Interface
- Operating Range: $V_{CC} = 3.135$ V to 5.25 V
- CMOS and TTL Compatible Control Inputs
- Pin and Function Compatible with Motorola MC12430 and MPC9230
- 0°C to 70°C Ambient Operating Temperature (NBC12430)
- -40°C to 85°C Ambient Operating Temperature (NBC12430A)
- Pb-Free Packages are Available

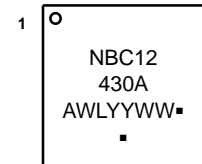
MARKING DIAGRAMS



**LQFP-32
FA SUFFIX
CASE 561AB**



1 32



- x = Blank or A
- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 16 of this data sheet.

NBC12430, NBC12430A

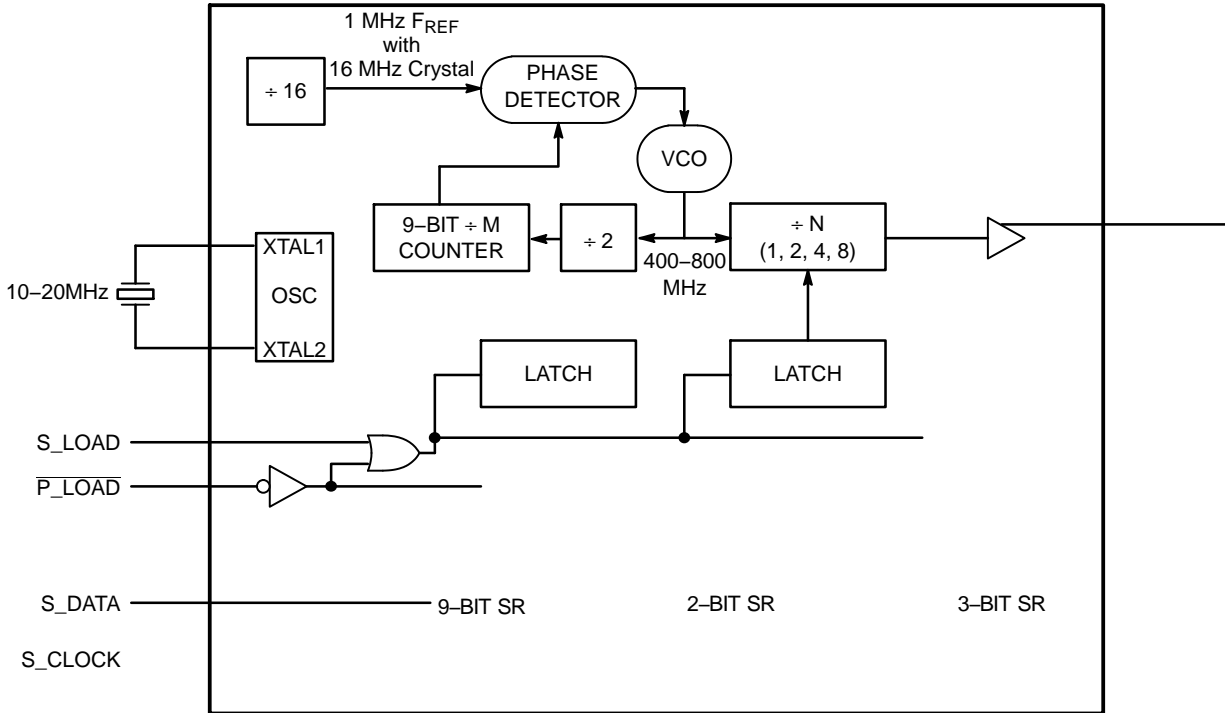


Figure 1. Block Diagram

NBC12430, NBC12430A

The following gives a brief description of the functionality of the NBC12430 and NBC12430A Inputs and Outputs. Unless explicitly stated, all inputs are CMOS/TTL compatible with either pullup or pulldown resistors. The PECL outputs are capable of driving two series terminated 50 Ω transmission lines on the incident edge.

Table 3. PIN FUNCTION DESCRIPTION

Pin Name	Function	Description
INPUTS		
XTAL1, XTAL2	Crystal Inputs	These pins form an oscillator when connected to an external series-resonant crystal.
S_LOAD*	CMOS/TTL Serial Latch Input (Internal Pulldown Resistor)	This pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH; thus, the data must be stable on the HIGH-to-LOW transition of S_LOAD for proper operation.
S_DATA*	CMOS/TTL Serial Data Input (Internal Pulldown Resistor)	This pin acts as the data input to the serial configuration shift registers.

S_CLOCK*

Table 4. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 k Ω
Internal Input Pullup Resistor	37.5 k Ω
ESD Protection Human Body Model Machine Model Charged Device Model	> 2 kV > 150 V > 1 kV
Moisture Sensitivity (Note 1) LQFP QFN	Pb-Free Pkg Level 2 Level 1
Flammability Rating Oxygen Index: 28 to 34'	UL 94 V-0 @ 0.125 in
Transistor Count	2011
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note [AND8003/D](#).

Table 5. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	Positive Supply	GND = 0 V		6	V
V _I	Input Voltage	GND = 0 V	V _I ≤ V _{CC}	6	V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
T _A	Operating Temperature Range				

NBC12430, NBC12430A

NBC12430, NBC12430A

Table 8. AC CHARACTERISTICS ($V_{CC} = 3.135\text{ V to }5.25\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C to }70^\circ\text{C}$ (NBC12430), $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (NBC12430A))
(Note 7)

Symbol	Characteristic	Condition	Min	Max	Unit
F_{MAXI}	Maximum Input Frequency S_CLOCK XTAL Oscillator FREF_EXT (Note 8)	(Note 6)	10 10	10 20 100	MHz
F_{MAXO}	Maximum Output Frequency VCO (Internal) F_{OUT}		400 50	800 800	MHz
t_{LOCK}	Maximum PLL Lock Time			10	ms
$t_{jitter(pd)}$	Period Jitter (RMS) (1 σ)	50 MHz $\leq f_{OUT} < 100$ MHz 100 MHz $\leq f_{OUT} < 800$ MHz		8 5	ps
$t_{jitter(cyc-cyc)}$	Cycle-to-Cycle Jitter (Peak-to-Peak) (8 σ)	50 MHz $\leq f_{OUT} < 100$ MHz 100 MHz $\leq f_{OUT} < 800$ MHz		± 40 ± 20	ps
t_s	Setup Time S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to P_LOAD		20 20 20		ns
t_h	Hold Time S_DATA to S_CLOCK M, N to P_LOAD		20 20		ns
tpw_{MIN}	Minimum Pulse Width S_LOAD P_LOAD		50 50		ns
DCO	Output Duty Cycle		47.5	52.5	%
t_r, t_f	Output Rise/Fall F_{OUT}	20%–80%	175	425	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfp/m.

6. 10 MHz is the maximum frequency to load the feedback divide registers. S_CLOCK can be switched at higher frequencies when used as a test clock in TEST_MODE 6.
7. $F_{OUT}/\overline{F_{OUT}}$ and TEST outputs are terminated through a 50 Ω resistor to $V_{CC} - 2.0\text{ V}$.
8. Maximum frequency on FREF_EXT is a function of setting the appropriate M counter value for the VCO to operate within the valid range of $400\text{ MHz} \leq f_{VCO} \leq 800\text{ MHz}$. (See Table 11).

APPLICATIONS INFORMATION

Using the On-Board Crystal Oscillator

The NBC12430 and NBC12430A feature a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large load capacitors per Figure 7 (do not use crystal load caps). The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs, the user is advised to mount the crystal as close to the device as possible to avoid any board level parasitics. To facilitate co-location, surface mount crystals are recommended, but not required. Because the series resonant design is affected by capacitive loading on the crystal terminals, loading variation introduced by crystals from different vendors could be a potential issue. For crystals with a higher shunt capacitance, it may be required to place a resistance, optional R_{shunt} , across the terminals to suppress the third harmonic. Although typically not required, it is a good idea to layout the PCB with the provision of adding this external resistor. The resistor value will typically be between 500 Ω and 1 k Ω .

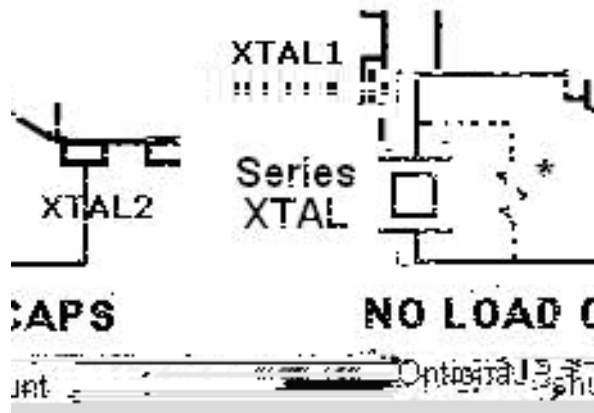


Figure 7. Crystal Application

The oscillator circuit is a series resonant circuit and thus, for optimum performance, a series resonant crystal should be used. Unfortunately, most crystals are characterized in a parallel resonant mode. Fortunately, there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result, a parallel resonant crystal can be used with the device with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant

NBC12430, NBC12430A

impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

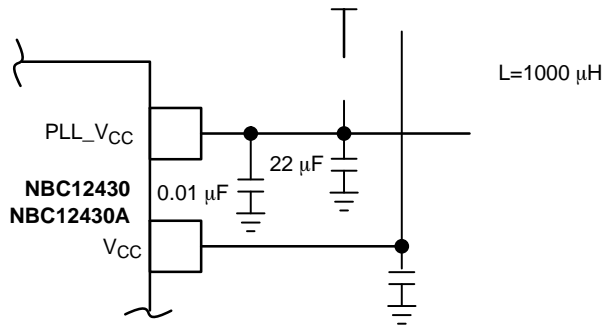


Figure 8. Power Supply Filter

NBC12430, NBC12430A

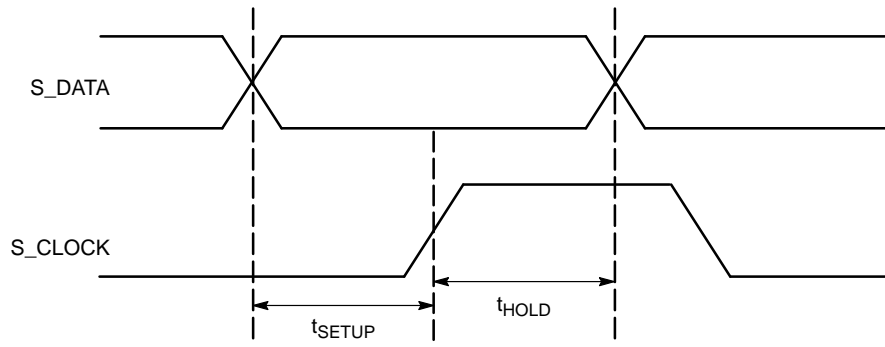


Figure 13. Setup and Hold

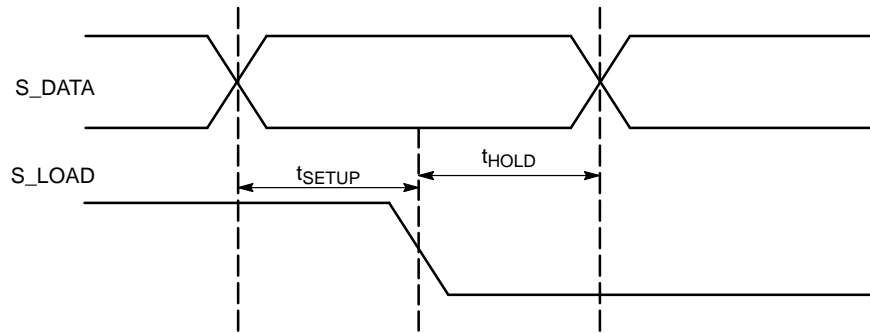


Figure 14. Setup and Hold

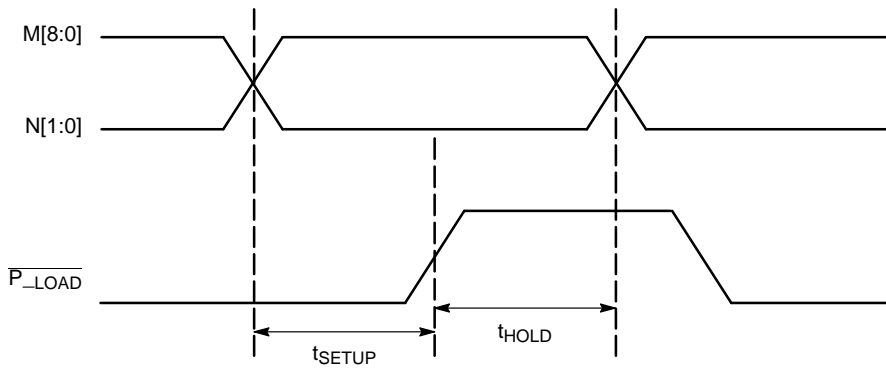


Figure 15. Setup and Hold

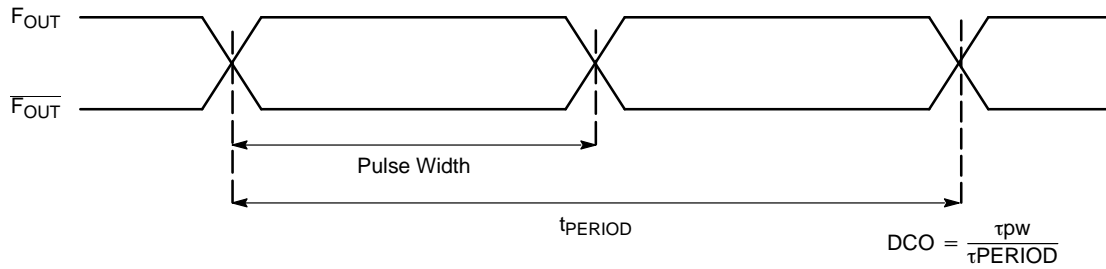


Figure 16. Output Duty Cycle

NBC12430, NBC12430A

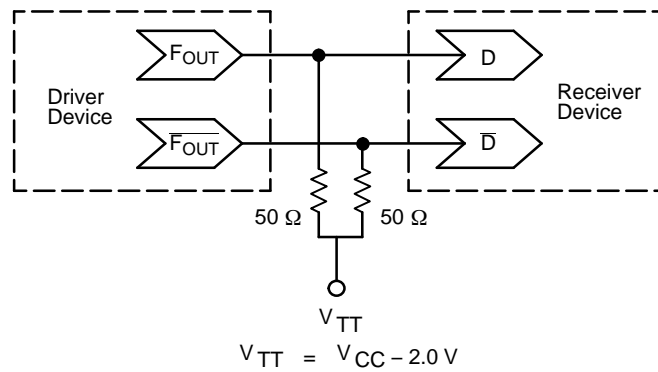


Figure 17. Typical Termination for Output Driver and Device Evaluation
(See Application Note [AND8020](#) – Termination of ECL Logic Devices.)

ORDERING INFORMATION

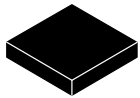
Device	Package	Shipping [†]
NBC12430FAR2G	LQFP-32 (Pb-Free)	2000 / Tape & Reel
NBC12430AMNG	QFN-32 (Pb-Free)	74 Units / Tube

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

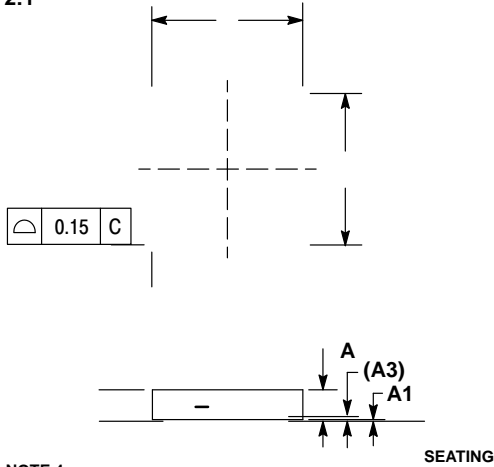
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QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

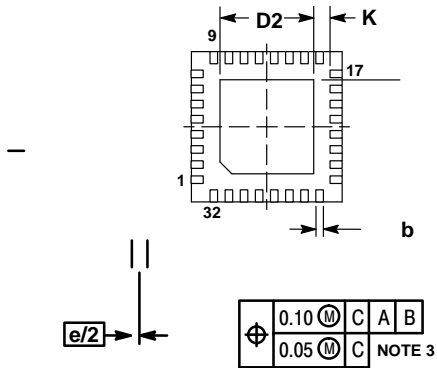
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SCALE 2:1



NOTE 4

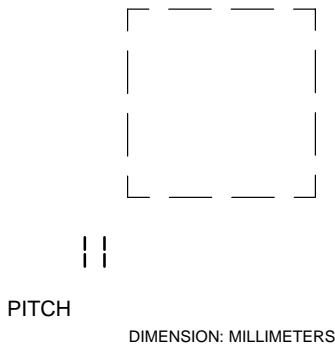
	MAX
A1	0.80 1.00
A3	0.20 REF 0.05
b	0.18 0.30
D	5.00 BSC
D2	2.95 3.25
E	5.00 BSC
E2	2.95 3.25
e	0.50 BSC
K	0.20
L	0.30 0.50
L1	0.15



XXXXXXXXXX
XXXXXXXXXX
AWLYYYWW■

■Free indicator, "G" or

RECOMMENDED



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