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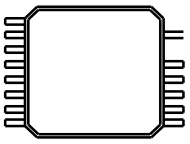
3.3 V/5 V Programmable PLL Synthesized Clock Generator

25 MHz to 400 MHz

NBC12429, NBC12429A

LQFP−32
FA SUFFIX
CASE 561AB

MARKING DIAGRAMS



Description

The NBC12429 and NBC12429A are general purpose, Phase−Lock−Loop (PLL) based synthesized clock sources. The VCO will operate over a frequency range of 200 MHz to 400 MHz. The VCO frequency is sent to the N−output divider, where it can be configured to provide division ratios of 1, 2, 4, or 8. The VCO and output frequency can be programmed using the parallel or serial interfaces to the configuration logic. Output frequency steps of 125 kHz, 250 kHz, 500 kHz, or 1.0 MHz can be achieved using a 16 MHz crystal, depending on the output dividers. The PLL loop filter is fully integrated and does not require any external components.

Features

- Best−in−Class Output Jitter Performance, ±20 ps Peak−to−Peak
- 25 MHz to 400 MHz Programmable Differential PECL Outputs
- Fully Integrated Phase−Lock−Loop with Internal Loop Filter
- Parallel Interface for Programming Counter and Output Dividers During Powerup
- Minimal Frequency Overshoot
- Serial 3−Wire Programming Interface
- Crystal Oscillator Interface
- Operating Range: V_{CC} = 3.135 V to 5.25 V
- CMOS and TTL Compatible Control Inputs
- Pin and Function Compatible with Motorola MC12429 and MPC9229
- 0°C to 70°C Ambient Operating Temperature (NBC12429)
- −40°C to 85°C Ambient Operating Temperature (NBC12429A)
- These Devices are Pb−Free and are RoHS Compliant

The following gives a brief description of the functionality of the NBC12429 and NBC12429A Inputs and Outputs. Unless explicitly stated, all inputs are CMOS/TTL compatible with either pullup or pulldown resistors. The PECL outputs are capable of driving two series terminated 50 Ω transmission lines on the incident edge.

Table 3. PIN FUNCTION DESCRIPTION

Pin Name	Function	Description
INPUTS		
XTAL1, XTAL2	Crystal Inputs	These pins form an oscillator when connected to an external series−resonant crystal.
S_LOAD*	CMOS/TTL Serial Latch Input (Internal Pulldown Resistor)	This pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH; thus, the data must be stable on the HIGH−to−LOW transition of S_LOAD for proper operation.
S_DATA*	CMOS/TTL Serial Data Input (Internal Pulldown Resistor)	This pin acts as the data input to the serial configuration shift registers.
S_CLOCK*	CMOS/TTL Serial Clock Input (Internal Pulldown Resistor)	This pin serves to clock the serial configuration shift registers. Data from S_DATA is sampled on the rising edge.
$\overline{\text{P\_LOAD}}$**	CMOS/TTL Parallel Latch Input (Internal Pullup Resistor)	This pin loads the configuration latches with the contents of the parallel inputs. The latches will be transparent when this signal is LOW; therefore, the parallel data must be stable on the LOW−to−HIGH transition of $\overline{\text{P\_LOAD}}$ for proper operation.

Table 4. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 kΩ
Internal Input Pullup Resistor	37.5 kΩ
ESD Protection Human Body Model Machine Model Charged Device Model	 > 2 kV > 150 V > 1 kV
Moisture Sensitivity (Note 1)	Pb−Free Pkg
LQFP QFN	Level 2 Level 1
Flammability Rating Oxygen Index: 28 to 34	 UL 94 V−0 @ 0.125 in
Transistor Count	2035
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 5. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Supply	GND = 0 V		6	V
V_I	Input Voltage	GND = 0 V	$V_I \le V_{CC}$	6	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range NBC12429 NBC12429A			 0 to 70 −40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	LQFP−32 LQFP−32	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	LQFP−32	12 to 17	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	QFN−32 QFN−32	31 27	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	2S2P	QFN−32	12	°C/W
T_{sol}	Wave Solder (Pb−Free)	<3 sec @ 260°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 6. DC CHARACTERISTICS (V_{CC} = 3.3 V ±5%; T_A = 0°C to 70°C (NBC12429), T_A = −40°C to 85°C (NBC12429A))

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IH} LVCMOS/ LVTTL	Input HIGH Voltage	V_{CC} = 3.3 V	2.0			V

Table 8. AC CHARACTERISTICS (V_{CC} = 3.125 V to 5.25 V; T_A = 0°C to 70°C (NBC12429), T_A = −40°C to 85°C (NBC12429A)) (Note 6)

Symbol	Characteristic		Condition	Min	Max	Unit
F_{MAXI}	Maximum Input Frequency	S_CLOCK Xtal Oscillator	(Note 7)	 10	10 20	MHz
F_{MAXO}	Maximum Output Frequency	VCO (Internal) F_{OUT}		200 25	400 400	MHz
$t_{jitter(pd)}$	Period Jitter @ 3.3 V 10000 WFMS (See Table 13 for Typical Values)		25 MHz < f_{OUT} < 100 MHz, M = 200 25 MHz < f_{OUT} < 100 MHz, M = 300 25 MHz < f_{OUT} < 100 MHz, M = 400 100 MHz < f_{OUT} < 400 MHz, M = 200 100 MHz < f_{OUT} < 400 MHz, M = 300 100 MHz < f_{OUT} < 400 MHz, M = 400 25 MHz < f_{OUT} < 100 MHz, M = 200 25 MHz < f_{OUT} 25 MHz < f		25 9.0 6.0 9.0 5.0 4.0	ps_{RMS}

Table 8. AC CHARACTERISTICS (V_{CC} = 3.125 V to 5.25 V; T_A = 0°C to 70°C (NBC12429), T_A = −40°C to 85°C (NBC12429A)) (Note 6)

Symbol	Characteristic		Condition	Min	Max	Unit
t_s	Setup Time	S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to $\overline{\text{P\_LOAD}}$		20 20 20		ns
t_h	Hold Time	S_DATA to S_CLOCK M, N to $\overline{\text{P\_LOAD}}$		20 20		ns
t_{pwMIN}	Minimum Pulse Width	S_LOAD $\overline{\text{P\_LOAD}}$		50 50		ns
DCO	Output Duty Cycle			47.5	52.5	%
t_r, t_f	Output Rise/Fall	F_{OUT}	20%−80%	175	425	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

6. $F_{OUT}/\overline{F_{OUT}}$ outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 V.
7. 10 MHz is the maximum frequency to load the feedback divide registers. S_CLOCK can be switched at higher frequencies when used as a test clock in TEST_MODE 6.

PROGRAMMING INTERFACE

Programming the NBC12429 and NBC12429A is accomplished by properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can by represented by this formula:

$$FOUT = (F_{XTAL} \div 16) \times M \div N \quad \text{(eq. 1)}$$

where F_{XTAL} is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be $200 \leq M \leq 400$ for a 16 MHz input reference.

Assuming that a 16 MHz reference frequency is used the above equation reduces to:

$$F_{OUT} = M \div N \quad \text{(eq. 2)}$$

Substituting the four values for N (1, 2, 4, 8) yields:

Table 10. Programmable Output Divider Function

N1	N0	N Divider	F_{OUT}	Output Frequency Range (MHz)*	F_{OUT} Step
0	0	÷1	M	200−400	

Most of the signals available on the TEST output pin are useful only for performance verification of the device itself. However, the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110, the device is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the F_{OUT} differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving F_{OUT} directly gives the user more control on the test clocks

APPLICATIONS INFORMATION

Using the On−Board Crystal Oscillator

The NBC12429 and NBC12429A feature a fully

increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

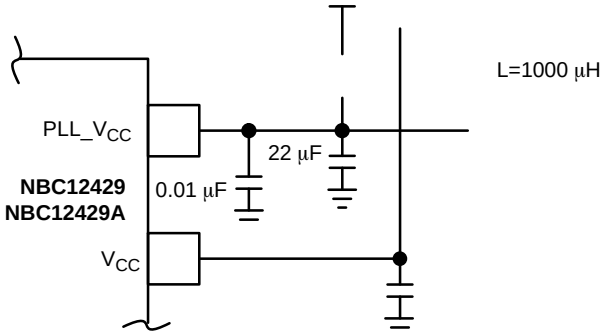


Figure 8. Power Supply Filter

Table 13. TYPICAL JITTER PERFORMANCE, 3.3 V, 25°C with 16 MHz Crystal Input at Selected M and N Values

	M Value	200	200	200	200	300	300	300	300	400	400	400	400
	N Value	1	2	4	8	1	2	4	8	1	2	4	8
JITTER	F												

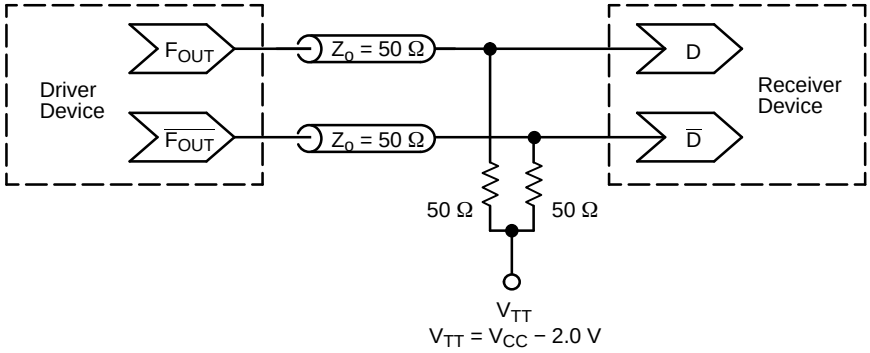


Figure 14. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1405/D − ECL Clock Distribution Techniques

AN1406/D − Designing with PECL (ECL at +5.0 V)

AN1503/D − ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D − Metastability and the ECLinPS Family

AN1568/D − Interfacing Between LVDS and ECL

AN1672/D − The ECL Translator Guide

AND8001/D − Odd Number Counters Design

AND8002/D − Marking and Date Codes

AND8020/D − Termination of ECL Logic Devices

AND8066/D − Interfacing with ECLinPS

AND8090/D − AC Characteristics of ECL Devices