

# 1.8 V/2.5 V Differential 2 x 2 Crosspoint Switch with CML Outputs Clock/Data Buffer/Translator

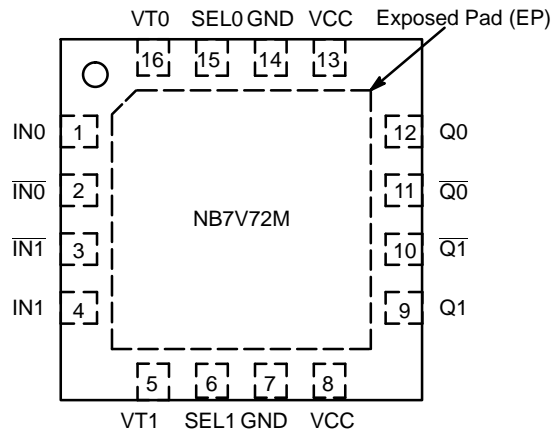
Multi-Level Inputs w/ Internal Termination

## NB7V72M

### Description

The NB7V72M is a high bandwidth, low voltage, fully differential 2 x 2 crosspoint switch with CML outputs. The NB7V72M design is optimized for low skew and minimal jitter as it produces two identical copies of Clock or Data operating up to 5 GHz or 6.5 Gb/s, respectively. As such, the NB7V72M is ideal for SONET, GigE, Fiber Channel, Backplane and other clock/data distribution applications. The differential  $\overline{IN}/\overline{IN}$  inputs incorporate internal 50  $\Omega$  termination resistors and will accept LVPECL, CML, or LVDS logic levels (see Figure 10). The 16 mA differential CML outputs provide matching internal 50  $\Omega$  terminations and produce 400 mV output swings when externally terminated with a 50

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**Table 1. INPUT/OUTPUT SELECT TRUTH TABLE**

SEL0*	SEL1*	Q0	Q1
L	L	IN0	IN0
L	H	IN0	IN1
H	L	IN1	IN0
H	H	IN1	IN1

\*Defaults HIGH when left open

**Figure 2. Pin Configuration (Top View)**

**Table 2. PIN DESCRIPTION**

Pin	Name	I/O	Description
1	IN0	LVPECL, CML, LVDS Input	Noninverted Differential Input. (Note 1)
2	IN0 with a bar	LVPECL, CML, LVDS Input	Inverted Differential Input. (Note 1)

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Table 3. ATTRIBUTES

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**Table 5. DC CHARACTERISTICS, Multi-Level Inputs**  $V_{CC} = 1.71 \text{ V to } 2.625 \text{ V}$ ,  $GND = 0 \text{ V}$ ,  $T_A = -40^\circ\text{C to } +85^\circ\text{C}$  (Note 4)

Symbol
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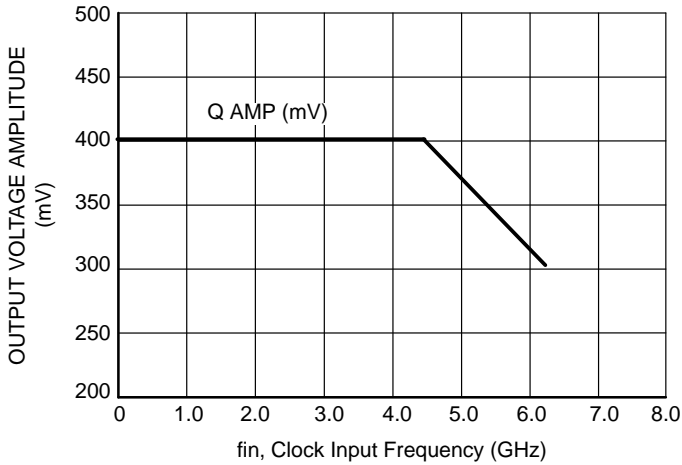
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**Table 6. AC CHARACTERISTICS**  $V_{CC} = 1.71\text{ V to }2.625\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (Note 10)

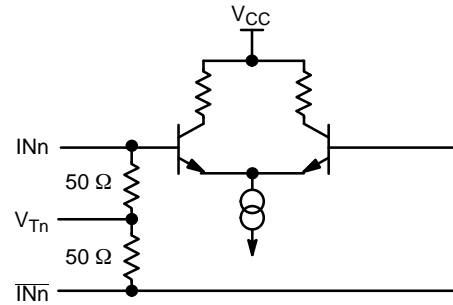
Symbol	Characteristic	Min	Typ	Max	Unit
$f_{MAX}$	Maximum Input Clock Frequency $V_{CC} = 2.5\text{ V}$ $V_{CC} = 1.8\text{ V}$	5 4.5			GHz
$f_{DATAMAX}$	Maximum Operating Data Rate (PRBS23)	6.5			Gbps
$V_{OUTPP}$	Output Voltage Amplitude (@ $V_{INPPmin}$ ) $f_{in} \leq 5\text{ GHz}$ (See Figures 3 and 10, Note 11)	200	400		mV
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Differential Outputs, @ 1GHz, Measured at Differential Cross-point $I_{Nn}/I_{N\bar{n}}$ to $Q_n/Q_{\bar{n}}$	110	150	200	ps
$t_{PLH\ TC}$	Propagation Delay Temperature Coefficient		50		$\Delta fs/^\circ C$
$t_{SKEW}$	Output-to-Output Skew (within device) (Note 12) Device-to-Device Skew ( $t_{pdmax} - t_{pdmin}$ )			30 50	ps
$t_{DC}$	Output Clock Duty Cycle (Reference Duty Cycle = 50%) $f_{in} \leq 5\text{ GHz}$	45	50	55	%
$t_{jitter}$	RJ – Output Random Jitter (Note 13) $f_{in} \leq 5\text{ GHz}$ DJ – Deterministic Jitter (Note 14) $\leq 9\text{ Gbps}$		0.5	0.8 10	ps RMS ps pk-pk
$V_{INPP}$	Input Voltage Swing (Differential Configuration) (Note 15)	100		1200	mV
$t_r$ , $t_f$	Output Rise/Fall Times @ 1 GHz (20% – 80%), $Q_n$ , $Q_{\bar{n}}$	20	30	50	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

10. Measured using a 400 mV source, 50% duty cycle clock source. All output loading with external  $50\ \Omega$  to  $V_{CC}$ . Input edge rates  $\geq 40\text{ ps}$  (20% – 80%).
11. Output voltage swing is a single-ended measurement operating in differential mode.
12. Skew is measured between outputs under identical transitions and conditions. Duty cycle skew is defined only for differential operation when the delays are measured from cross-point of the inputs to the cross-point of the outputs.
13. Additive RMS jitter with 50% duty cycle clock signal.
14. Additive Peak-to-Peak data dependent jitter with input NRZ data at PRBS23.
15. Input voltage swing is a single-ended measurement operating in differential mode.



**Figure 3. CLOCK Output Voltage Amplitude ( $V_{OUTPP}$ ) vs. Input Frequency ( $f_{in}$ ) at Ambient Temperature (Typ)**



**Figure 4. Input Structure**

**NB7V72M**

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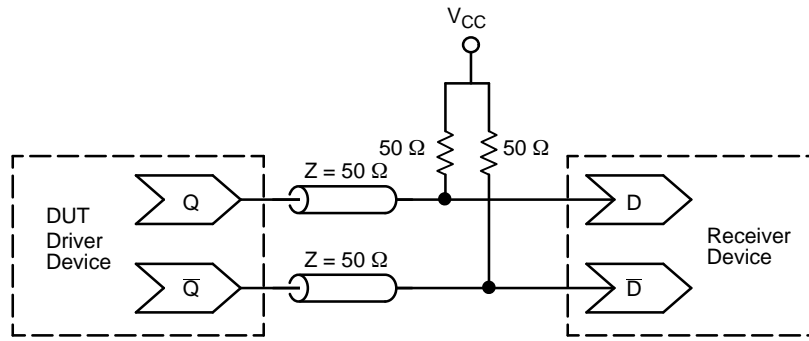
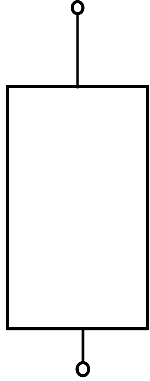


Figure 12. Typical Termination for CML Output Driver and Device Evaluation





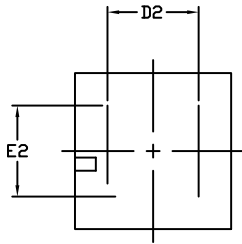
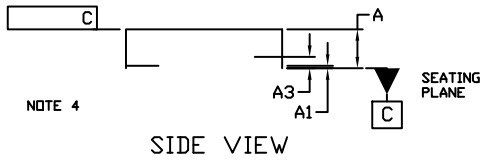
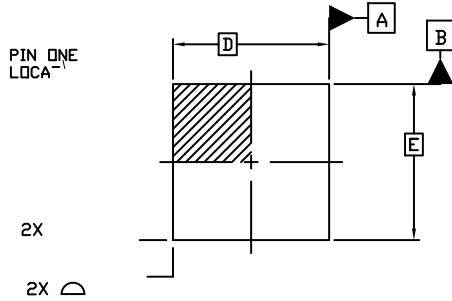




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SCALE 2:1

**QFN16 3x3, 0.5P**  
CASE 485G  
ISSUE G

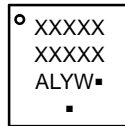
DATE 08 OCT 2021



NOTE 3

BOTTOM VIEW

**GENERIC MARKING DIAGRAM\***



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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