

2.5 V, 10 GH ÷4 Cl ck

Multi-Level Inputs w/ Internal Termination

NB7V33M

Description

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TM

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= Assembly Location Α

L = Wafer Lot

= Year

W = Work Weeh.45hese t9S7s4Jpp5110e0D12 0 0 1

Features

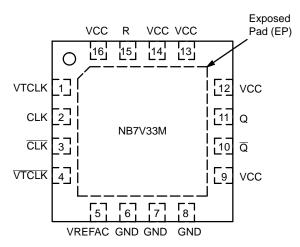


Figure 2. Pin Configuration (Top View)

Table 1. TRUTH TABLE

Table 5. DC CHARACTERISTICS POSITIVE CML OUTPUT $V_{CC} = 1.71 \text{ V}$ to 2.625 V; GND = 0 V; $T_A = -40 ^{\circ}\text{C}$ to $85 ^{\circ}\text{C}$ (Note 5)

Symbol	Characteristic		Min	Тур	Max	Unit
POWER	SUPPLY CURRENT					
I _{CC}		CC = 2.5 V ± 5% CC = 1.8 V ± 5%		95 85	115 100	mA
CML OU	TPUTS					
V _{OH}	Output HIGH Voltage (Note 6)	VCC = 2.5 V VCC = 1.8 V	V _{CC} – 30 2470 1770	V _{CC} - 10 2490 1790	V _{CC} 2500 1800	mV
V _{OL}	Output LOW Voltage (Note 6)	Vcc = 2.5 V Vcc = 1.8 V	V _{CC} - 650 1850 V _{CC} - 600 1200	V _{CC} - 550 1950 V _{CC} - 500 1300	V _{CC} - 450 2050 V _{CC} - 400 1400	mV
DIFFERE	ENTIAL INPUTS DRIVEN SINGLE-ENDED (Note 7) (Fig	ures 5 & 6)				
V_{th}	Input Threshold Reference Voltage Range (Note 8)		1050		V _{CC} – 100	mV
V_{IH}	Single-ended Input HIGH Voltage		V _{th} + 100		V _{CC}	mV
V_{IL}	Single-ended Input LOW Voltage		GND		V _{th} – 100	mV
V_{ISE}	Single-ended Input Voltage (V _{IH} - V _{IL})		200		1200	mV
VREFAC						
V _{REFAC}	Output Reference Voltage @100 μA for Capacitor- Cou	upled Inputs, Only $V_{CC} = 2.5 \text{ V}$ $V_{CC} = 1.8 \text{ V}$	V _{CC} - 850 V _{CC} - 750		V _{CC} - 500 V _{CC} - 450	mV
DIFFERE	ENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 7	& 8) (Note 9)				
V_{IHD}	Differential Input HIGH Voltage		1100		V _{CC}	mV
V_{ILD}	Differential Input LOW Voltage		GND		V _{CC} – 100	mV
V_{ID}	Differential Input Voltage (V _{IHD} – V _{ILD})		100		1200	mV
V_{CMR}	Input Common Mode Range (Differential Configuration, Note 10) (Figure 9)		1050		V _{CC} - 50	mV
I _{IH}	Input HIGH Current (VTx/VTx Open)		-150		150	μΑ
I _{IL}	Input LOW Current (VTx/VTx Open)		-150		150	μΑ
CONTRO	DL INPUT (Reset pin)					
V _{IH}	Input HIGH Voltage for Control Pin		V _{CC} – 200		V _{CC}	mV
V_{IL}	Input LOW Voltage for Control Pin		GND		200	mV
I _{IH}	Input HIGH Current		-150		150	μΑ
I _{IL}	Input LOW Current		-150		150	μΑ
TERMIN	ATION RESISTORS					
R _{TIN}	Internal Input Termination Resistor		45	50	55	Ω
R _{TOUT}	Internal Output Termination Resistor		45	50	55	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

^{5.} Input and output parameters vary 1:1 with V_{CC}.
6. CML outputs loaded with 50–CC

Table 6. AC CHARACTERISTICS $V_{CC} = 1.71 \text{ V}$ to 2.625 V; GND = 0 V; $T_A = -40 ^{\circ}\text{C}$ to $85 ^{\circ}\text{C}$ (Note 11)

Symbol Characteristic Min Typ Max U

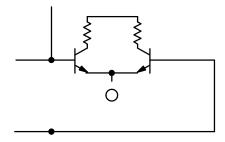
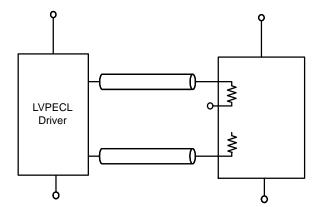


Figure 4. Input Structure



DEVICE ORDERING INFORMATION

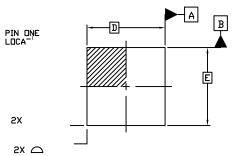
Device	Package	Shipping [†]
NB7V33MMNG	QFN-16 (Pb-Free)	123 Units / Rail
NB7V33MMNHTBG	QFN-16 (Pb-Free)	100 / Tape & Reel
NB7V33MMNTXG	QFN-16 (Pb-Free)	3,000 / Tape & Reel

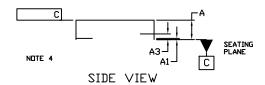
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging

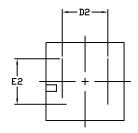


QFN16 3x3, 0.5P CASE 485G ISSUE G

DATE 08 OCT 2021







NOTE 3

BOTTOM VIEW

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code A = Assembly Location

L = Wafer Lot Y = Year W = Work Week ■ Pb-Free Package

(Note: Microdot may be in either location)

^{*}This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

