2.5 V / 3.3 V Differential 4:1 Mux Input to 1:2 LVPECL Clock/Data Fanout / Translator

Multi−Level Inputs w/ Internal Termination

NB7L572

The NB7L572 is a high performance differential 4:1 Clock/Data input multiplexer and a 1:2 LVPECL Clock/Data fanout buffer. The INx/$\overline{\text{INx}}$ inputs includes internal 50 Ω termination resistors and will accept differential LVPECL, CML, or LVDS logic levels. The NB7L572 incorporates a pair of Select pins that will choose one of four differential inputs and will produce two identical LVPECL output copies of Clock or Data operating up to 7 GHz or 10 Gb/s, respectively. As such, NB7L572 is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock/Data distribution applications.

The NB7L572 INx/$\overline{\text{INx}}$ inputs, outputs and core logic are powered by a 2.5 V ±5% V or 3.3 V ±10% power supply. The two differential LVPECL outputs will swing 750 mV when externally terminated with a 50 Ω resistor to V_{CC} − 2 V, and are optimized for low skew and minimal jitter.

The NB7L572 is offered in a low profile 5x5 mm 32-pin QFN Pb-free package. Application notes, models, and support documentation are available at www.onsemi.com.

The NB7L572 is a member of the GigaComm™ family of high performance clock products.

Features

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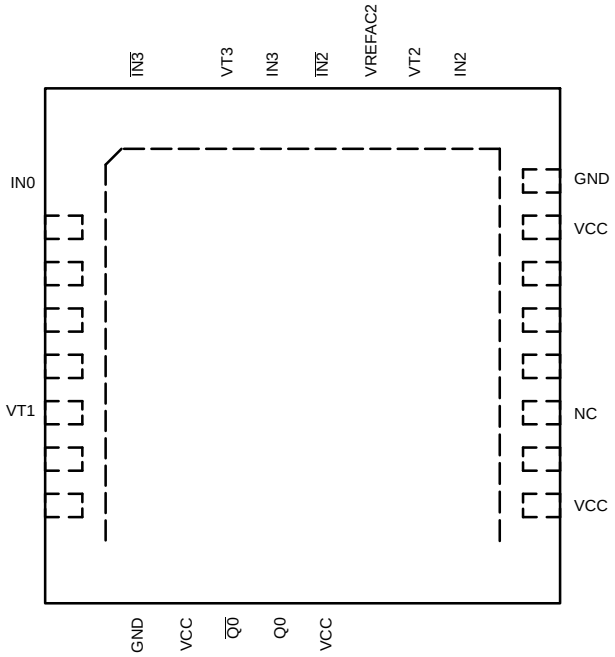


Figure 1. Pinout Configuration (Top View)

Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
1, 4 5, 8 25, 28 29, 32	IN0, $\overline{IN0}$ IN1, $\overline{IN1}$ IN2, $\overline{IN2}$ IN3, $\overline{IN3}$	LVPECL, CML, LVDS Input	Non−inverted, Inverted, Differential Clock or Data Inputs.
2, 6 26, 30	VT0, VT1 VT2, VT3		Internal 100 Ω Center−tapped Termination Pin for INx / $\overline{INx}$
15 18	SEL0 SEL1	LVTTL/LVCMOS Input	Input Select pins, default HIGH when left open through a 28k−Ω pull−up resistor. Input logic threshold is V_{CC}/2. See Select Function, Table 1.
14, 19	NC	−	No Connect
10, 13, 16 17, 20, 23	VCC	−	Positive Supply Voltage. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
11, 12 21, 22	$\overline{Q0}$, Q0 $\overline{Q1}$, Q1	LVPECL Output	Inverted, Non−inverted Differential Outputs.
9, 24	GND		Negative Supply Voltage, connected to Ground
3 7 27 31	VREFAC0 VREFAC1 VREFAC2 VREFAC3	−	Output Voltage Reference for Capacitor−Coupled Inputs
−	EP	−	The Exposed Pad (EP) on the QFN−

Table 3. ATTRIBUTES

Characteristic		Value
ESD Protection	Human Body Model Machine Model	> 4 kV > 150 V
Input Pullup Resistor (R_{PU})		28 kΩ
Moisture Sensitivity (Note 3)	QFN32	Level 1
Flammability Rating Oxygen Index: 28 to 34		UL 94 V−0 @ 0.125 in
Transistor Count		205
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		−0.5 to +4.0	V
V_{IN}	Positive Input Voltage	GND = 0 V		−0.5 to V_{CC} +0.5	V
V_{INPP}	Differential Input Voltage |IN – $\overline{IN}$|			1.89	V
I_{out}					

Table 5. DC CHARACTERISTICS POSITIVE LVPECL OUTPUT V_{CC} = 2.375 V to 3.6 V, GND = 0 V, TA = −40°C to +85°C (Note 6)

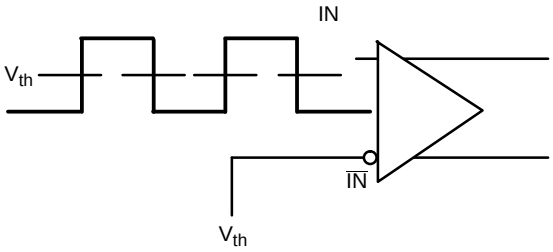
Symbol	Characteristic	Min	Typ	Max	Unit
POWER SUPPLY					
V_{CC}	Power Supply Voltage V_{CC} = 2.5V V_{CC} = 3.3 V	2.375 3.0	2.5 3.3	2.625 3.6	V
I_{CC}	Power Supply Current for V_{CC} (Inputs and Outputs Open)		90	110	mA
LVPECL OUTPUTS					
V_{OH}	Output HIGH Voltage (Note 6) V_{CC} = 2.5 V V_{CC} = 3.3 V	V_{CC} – 1145 1355 2155	V_{CC} – 900 1600 2400	V_{CC} – 825 1675 2475	mV
V_{OL}	Output LOW Voltage (Note 6) V_{CC} = 2.5 V V_{CC} = 3.3 V	V_{CC} – 2000 500 1300	V_{CC} – 1700 800 1600	V_{CC} – 1500 1000 1800	mV
DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE−ENDED (Figures 4 & 6) (Note 7)					
V_{IH}	Single−Ended Input HIGH Voltage	V_{th} + 100		V_{CC}	mV
V_{IL}	Single−Ended Input LOW Voltage	GND		V_{th} – 100	mV
V_{th}	Input Threshold Reference Voltage Range (Note 8)	1100		V_{CC} – 100	mV
V_{ISE}	Single−Ended Input Voltage (V_{IH} – V_{IL})	200		2400	mV
VREFAC					
$V_{REF−AC}$	Output Reference Voltage (100 μA Load)	V_{CC} – 1500	V_{CC} – 1200	V_{CC} – 1000	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 5 & 7) (Note 9)					
V_{IHD}	Differential Input HIGH Voltage (IN, $\overline{IN}$)	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage (IN, $\overline{IN}$)	0		V_{IHD} – 100	mV
V_{ID}	Differential Input Voltage (IN, $\overline{IN}$) (V_{IHD} – V_{ILD})	100		1200	mV
V_{CMR}	Input Common Mode Range (Differential Configuration, Note 10) (Figure 8)	800		V_{CC} – 50	mV
I_{IH}	Input HIGH Current IN/$\overline{IN}$ (VT IN/VT $\overline{IN}$ Open)	−150		150	μA
I_{IL}	Input LOW Current IN/$\overline{IN}$ (VT IN/VT $\overline{IN}$ Open)	−150		150	μA
CONTROL INPUT (SELx Pin)					
V_{IH}	Input HIGH Voltage for Control Pin	2.0		V_{CC}	V
V_{IL}	Input LOW Voltage for Control Pin	GND		0.8	V
I_{IH}	Input HIGH Current			40	μA
I_{IL}	Input LOW Current	−215		0	μA
TERMINATION RESISTORS					
R_{TIN}	Internal Input Termination Resistor (Measured from INx to VTx)	45	50	55	Ω

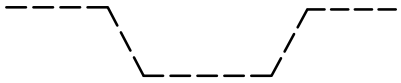
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

5. Input and Output parameters vary 1:1 with V_{CC}.
6. LVPECL outputs loaded with 50 Ω to V_{CC} − 2V for proper operation.
7. Vth, V_{IH}, $V_{IL,,}$ and V_{ISE} parameters must be complied with simultaneously.
8. Vth is applied to the complementary input when operating in single−ended mode.
9. V_{IHD}, $V_{ILD,}$ V_{ID} and V_{CMR} parameters must be complied with simultaneously.
10. V_{CMR} min varies 1:1 with GND, V_{CMR} max varies 1:1 with V_{CC}. The V_{CMR} range is referenced to the most positive side of the differential input signal.

Table 6. AC CHARACTERISTICS V_{CC} = 2.375 V to 3.6 V, GND = 0 V, TA = −40°C to +85°C (Note 11)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{MAX}					


IN
V_{th}
$\overline{IN}$
V_{th}



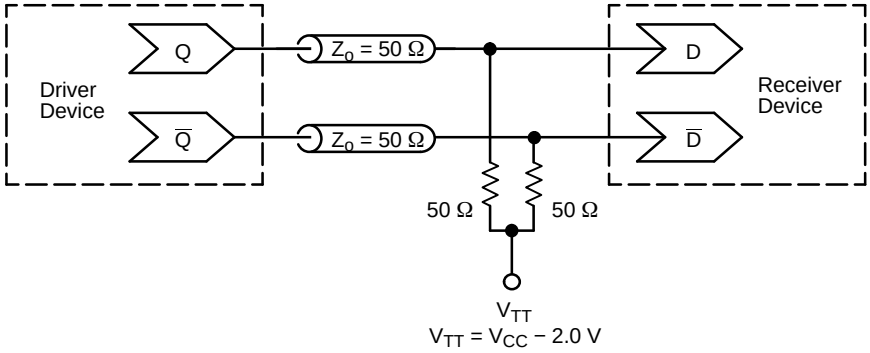
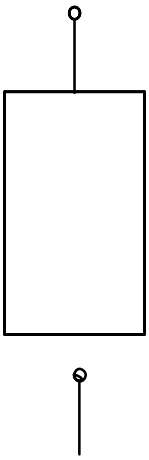


Figure 11. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)



ORDERING INFORMATION

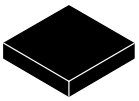
Device	Package	Shipping†
NB7L572MNG	QFN32 (Pb−Free)	74 Units / Tube
NB7L572MNR4G	QFN32 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

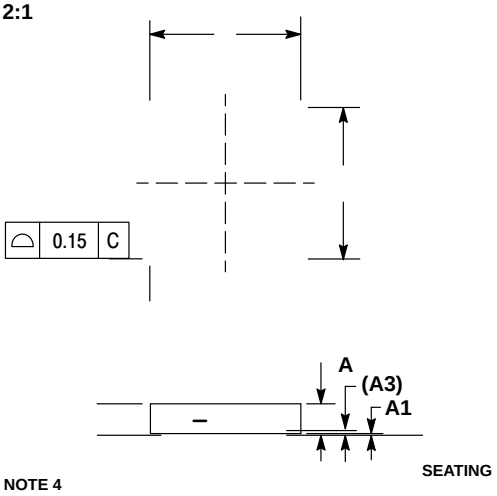
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

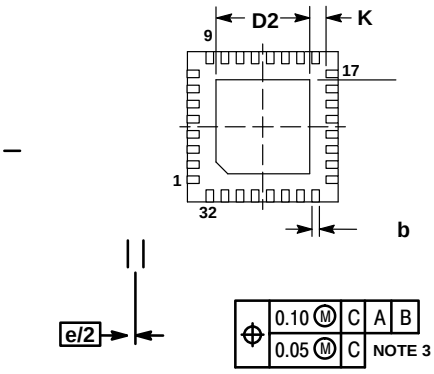
DATE 23 OCT 2013



SCALE 2:1



	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15



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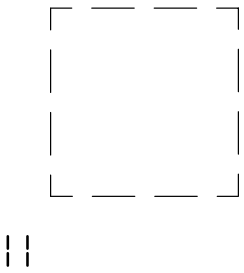
XXXXXXXX
AWLYYWW▪
▪Free indicator, “G” or

RECOMMENDED



PITCH

DIMENSION: MILLIMETERS

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