

# 2.5 V / 3.3 V Differential 2 X 2 Crosspoint Switch with CML Outputs

## Multi-Level Inputs w/ Internal Termination

### NB6L72M

#### Description

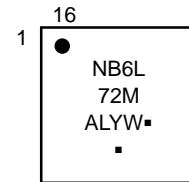
The NB6L72M is a clock or data high-bandwidth fully differential 2 x 2 Crosspoint Switch with internal source termination and CML output structure, optimized for low skew and minimal jitter. The differential inputs incorporate internal 50 Ω termination resistors and will accept LVPECL, CML, LVDS, LVCMOS, or LVTTTL logic levels. The SELECT inputs are single-ended and can be driven with LVCMOS/LVTTTL.

The 16 mA differential CML outputs provide matching internal 50 Ω terminations and 400 mV output swings when externally terminated with a 50 Ω resistor to V<sub>CC</sub>.

The device is offered in a small 3 mm x 3 mm 16-pin QFN package. The NB6L72M is a member of the ECLinPS MAX™

- Functionally Compatible with Existing 2.5 V / 3.3 V LVEL, LVEP, EP, and SG Devices
- -40°C to +85°C Ambient Operating Temperature
- These are Pb-Free Devices

#### MARKING DIAGRAM\*



- A = Assembly Location
  - L = Wafer Lot
  - Y = Year
  - W = Work Week
  - = Pb-Free Package
- (Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

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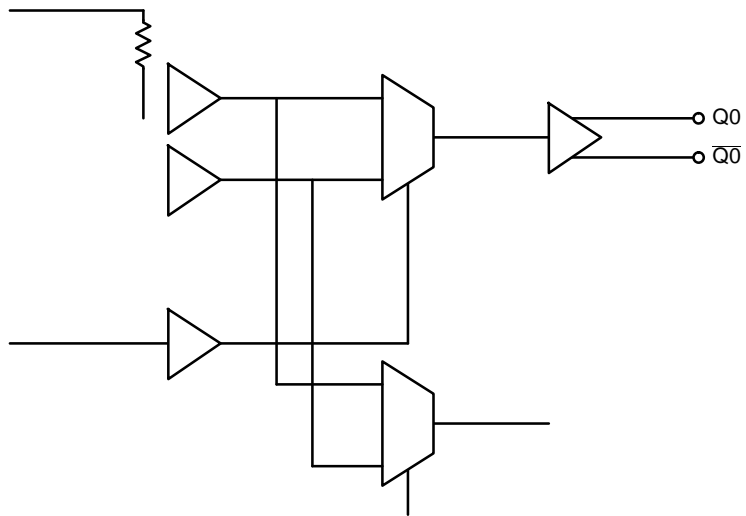
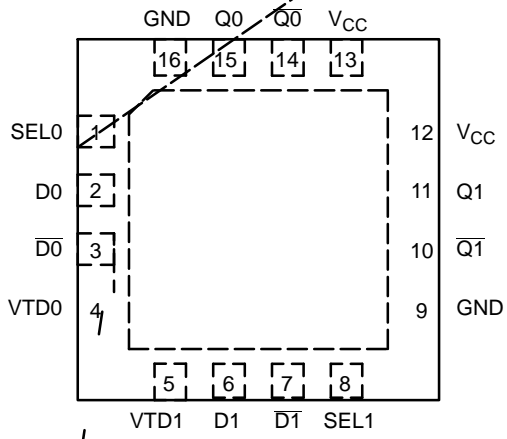


Figure 1. Logic/Block Diagram

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**NB6L72M**

**Table 5. DC CHARACTERISTICS, Multi-Level Inputs V**

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**Table 6. AC CHARACTERISTICS**  $V_{CC} = 2.375\text{ V to }3.63\text{ V}$ ,  $GND = 0\text{ V}$ , or  $V_{CC} = 0\text{ V}$ ,  $GND = -2.375\text{ V to }-3.63\text{ V}$ ,  
 $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ ; (Note 10)

Symbol	Characteristic	Min	Typ	Max	Unit
$V_{OUTPP}$	Output Voltage Amplitude (@ $V_{INPPmin}$ ) (Note 15) (See Figure 15)	$f_{in} \leq 3\text{ GHz}$	250	380	mV

f

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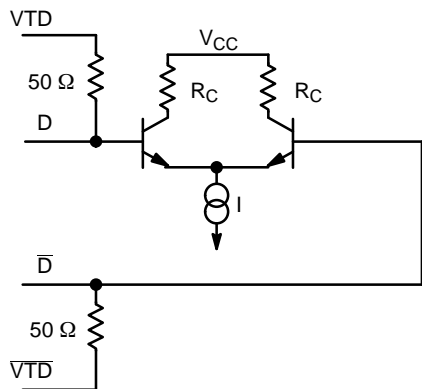


Figure 3. Input Structure

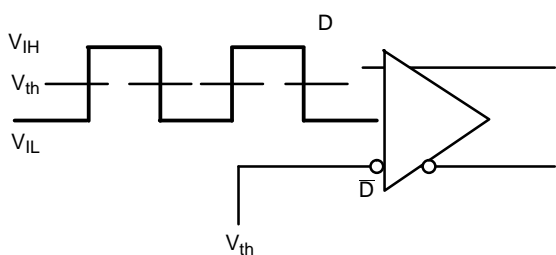


Figure 4. Differential Input Driven Single-Ended

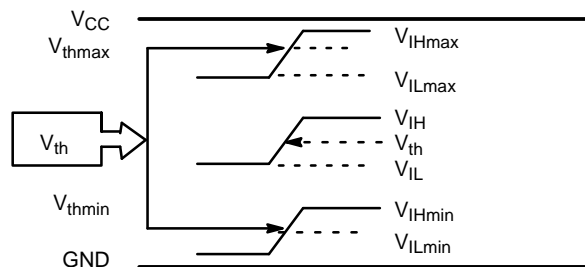


Figure 5.  $V_{th}$  Diagram

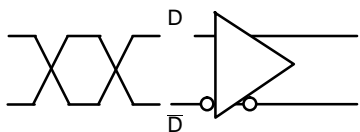


Figure 6. Differential Inputs Driven Differentially

Figure 7. Differential Inputs Driven Differentially

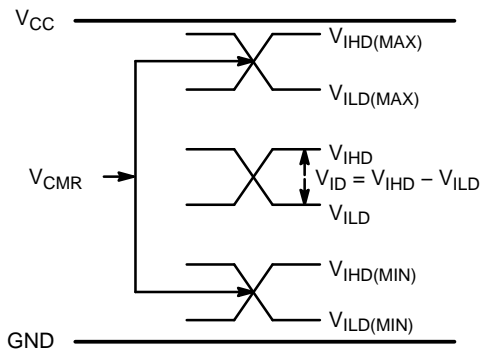
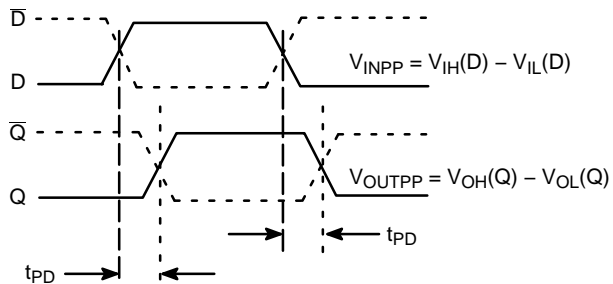
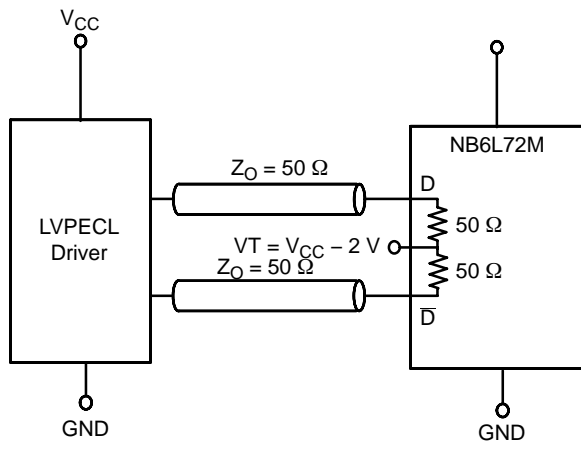


Figure 8.  $V_{CMR}$



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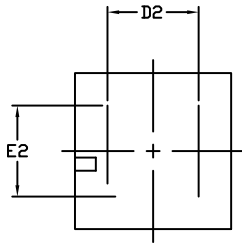
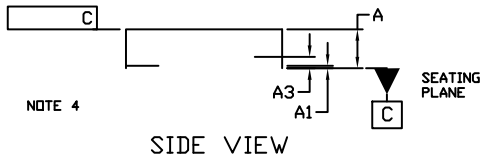
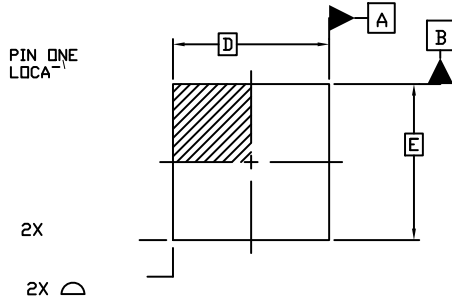
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1  
SCALE 2:1

**QFN16 3x3, 0.5P**  
CASE 485G  
ISSUE G

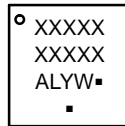
DATE 08 OCT 2021



BOTTOM VIEW

NOTE 3

**GENERIC MARKING DIAGRAM\***



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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