

# 2.5 V / 3.3 V Differential 2 X 2 Crosspoint Switch with LVPECL Outputs

## Multi-Level Inputs w/ Internal Termination

### NB6L72

#### Description

The NB6L72 is a clock or data high-bandwidth fully differential 2 x

# NB6L72

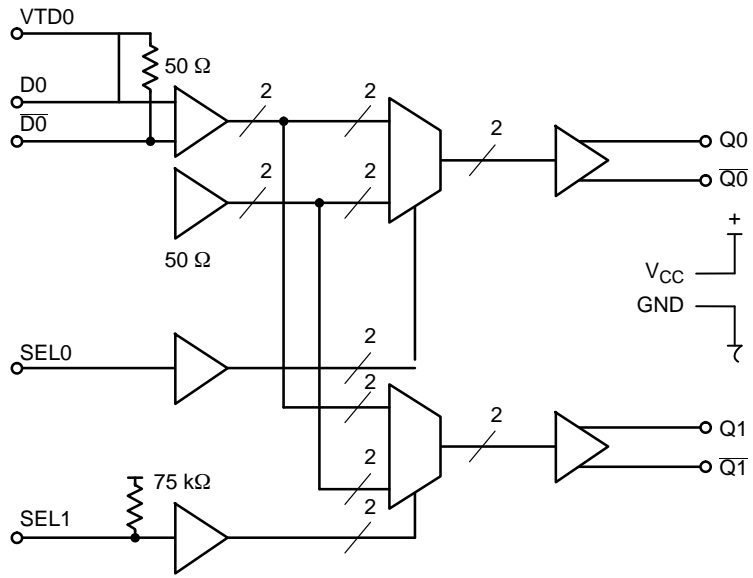


Figure 1. Logic/Block Diagram

# NB6L72

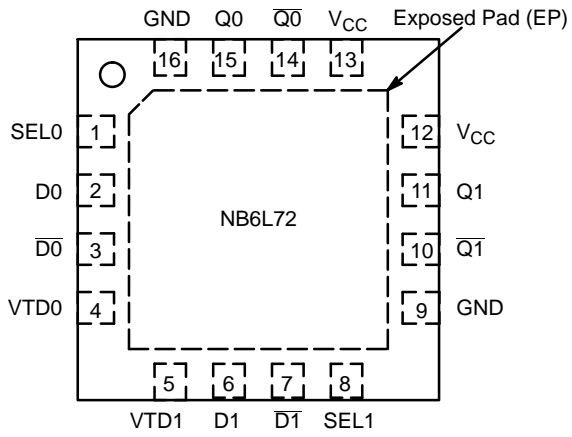


Figure 2. Pin Configuration (Top View)

Table 1. INPUT/OUTPUT SELECT TRUTH TABLE

SEL0*	SEL1*	Q0	Q1
L	L	D0	D0
H	L	D1	D0
L	H	D0	D1
H	H	D1	D1

\*Defaults HIGH when left open

Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
1	SEL0		

**NB6L72**



## NB6L72

**Table 5. DC CHARACTERISTICS, Multi-Level Inputs**  $V_{CC} = 2.375\text{ V to }3.63\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$

Symbol	Characteristic	Min	Typ	Max	Unit
<b>POWER SUPPLY CURRENT</b>					
$I_{CC}$	Power Supply Current (Inputs and Outputs Open)	40	60	80	mA
<b>LVPECL OUTPUTS (Notes 4 and 5)</b>					
$V_{OH}$	Output HIGH Voltage $V_{CC} = 3.3\text{ V}$ $V_{CC} = 2.5\text{ V}$	$V_{CC} - 1075$ 2225 1425	$V_{CC} - 950$ 2350 1550	$V_{CC} - 825$ 2475 1675	mV
$V_{OL}$	Output LOW Voltage $V_{CC} = 3.3\text{ V}$ $V_{CC} = 2.5\text{ V}$	$V_{CC} - 1825$ 1475 675	$V_{CC} - 1725$ 1575 775	$V_{CC} - 1625$ 1675 875	mV
<b>DIFFERENTIAL INPUT DRIVEN SINGLE-ENDED (see Figures 4 and 5) (Note 6)</b>					
$V_{th}$	Input Threshold Reference Voltage Range (Note 7)	1125		$V_{CC} - 150$	mV
$V_{IH}$	Single-ended Input HIGH Voltage	$V_{th} + 150$		$V_{CC}$	mV
$V_{IL}$	Single-ended Input LOW Voltage	GND		$V_{th} - 150$	mV
$V_{ISE}$	Single-ended Input Voltage Amplitude ( $V_{IH} - V_{IL}$ )	300		$V_{CC} - GND$	mV
<b>DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (see Figures 7 and 9)</b>					
$V_{IHD}$	Differential Input HIGH Voltage	1050		$V_{CC}$	mV
$V_{ILD}$	8 Tm-.e4675 I02.5575 491.3008 Tm-.0012 Tc7GH V				

Table 6. AC CHARACTERISTICS V

# NB6L72

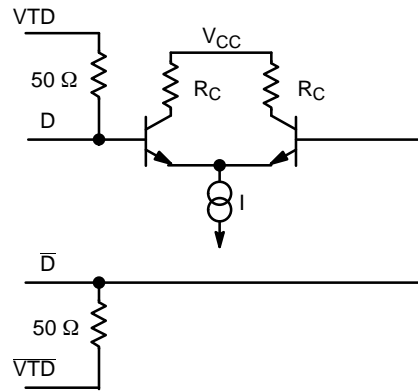


Figure 3. Input Structure

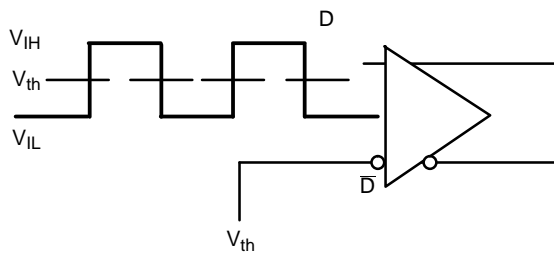
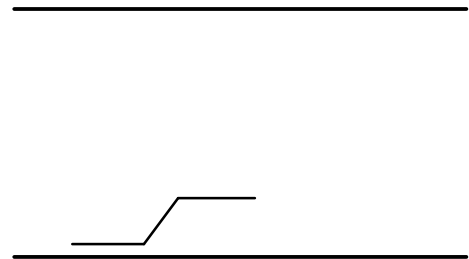


Figure 4. Differential Input Driven Single-Ended



# NB6L72

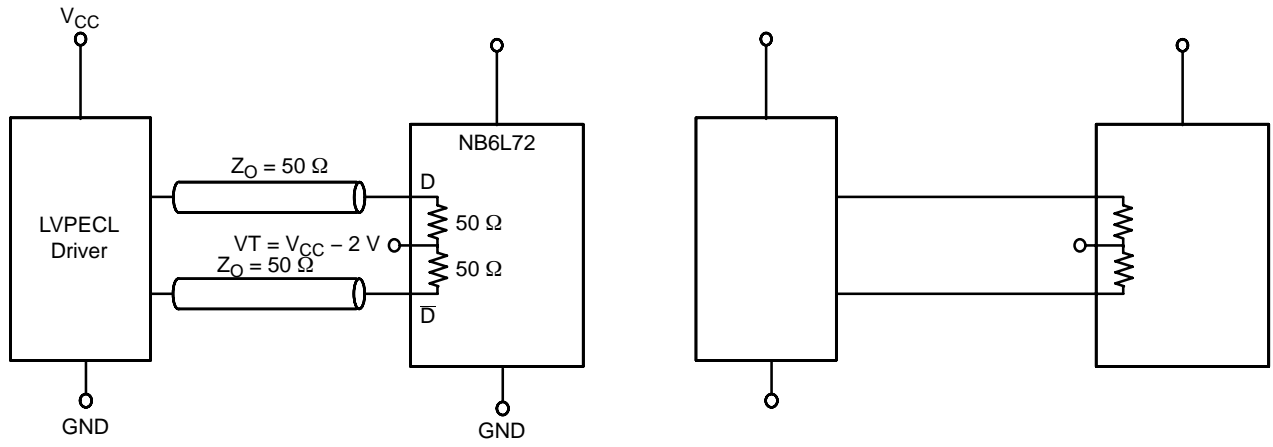
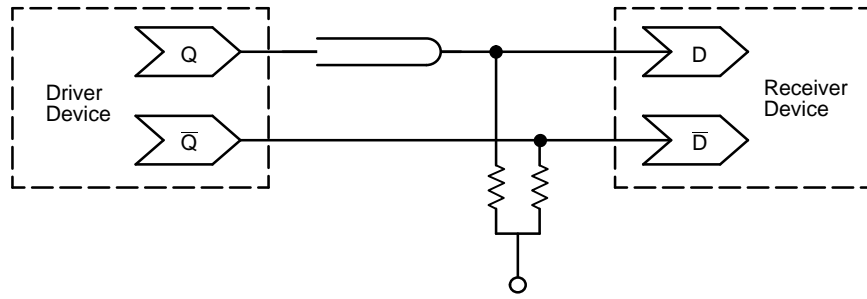


Figure 10. LVPECL Interface

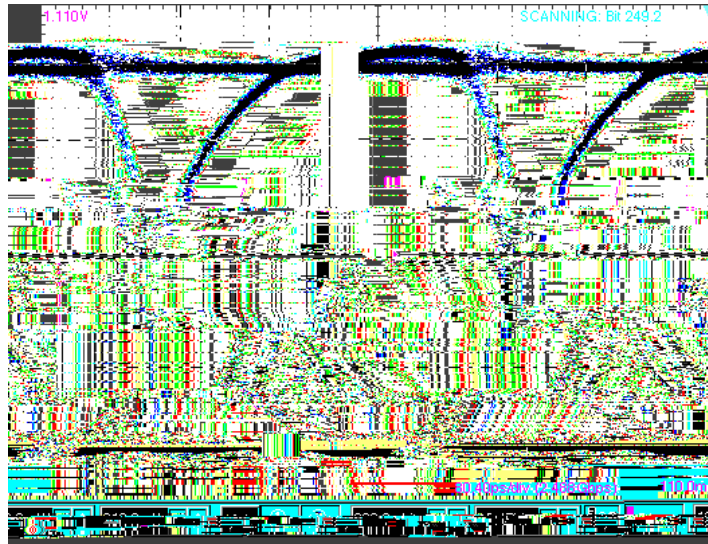


# NB6L72



**Figure 15. Typical Termination for Output Driver and Device Evaluation  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)**

# NB6L72



Total Jitter = 28 ps  
Device Jitter = 15 ps  
Input Jitter = 13 ps

Figure 18. Typical Output Wave Form – Data Signal PRBS 2<sup>23</sup>-1 Room Temperature, 75 mV Input Amplitude, 3 Gb/s (X-scale = 80 ps/DIV; y-Scale = 100 mV/DIV)

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NB6L72MNG	QFN-16 (Pb-free)	123 Units / Rail
NB6L72MNR2G	QFN-16 (Pb-free)	3000 / Tape & Reel

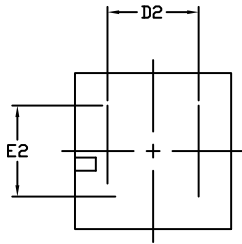
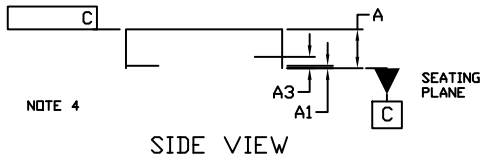
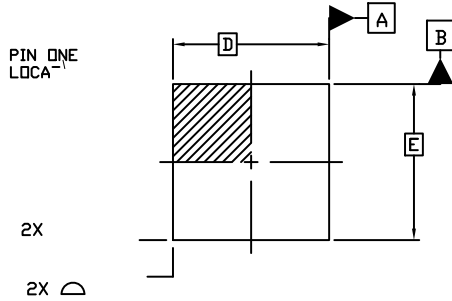
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



1  
SCALE 2:1

**QFN16 3x3, 0.5P**  
CASE 485G  
ISSUE G

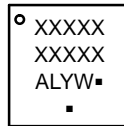
DATE 08 OCT 2021



NOTE 3

BOTTOM VIEW

**GENERIC MARKING DIAGRAM\***



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**onsemi**, **onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi**

---

---