2.5 V / 3.3 V Dual Channel Programmable Clock/Data Delay with Differential CML Outputs

Multi−Level Inputs w/ Internal Termination

NB6L295M

The NB6L295M is a Dual Channel Programmable Delay Chip designed primarily for Clock or Data de−skewing and timing adjustment. The NB6L295M is versatile in that two individual variable delay channels, PD0 and PD1, can be configured in one of two operating modes, a Dual Delay or an Extended Delay.

In the Dual Delay Mode, each channel has a programmable delay section which is designed using a matrix of gates and a chain of multiplexers. There is a fixed minimum delay of 3.2 ns per channel.

The Extended Delay Mode amounts to the additive delay of PD0 plus PD1 and is accomplished with the Serial Data Interface MSEL bit set High. This will internally cascade the output of PD0 into the input of PD1. Therefore, the Extended Delay path starts at the IN0/$\overline{\text{IN0}}$ inputs, flows through PD0, cascades to the PD1 and outputs through Q1/$\overline{\text{Q1}}$. There is a fixed minimum delay of 6.0 ns for the Extended Delay Mode.

The required delay is accomplished by programming each delay channel via a 3−pin Serial Data Interface, described in the application section. The digitally selectable delay has an increment resolution of typically 11 ps with a net programmable delay range of either 0 ns to 6 ns per channel in Dual Delay Mode; or from 0 ns to 11.2 ns for the Extended Delay Mode.

The Multi−Level Inputs can be driven directly by differential LVPECL, LVDS or CML logic levels; or by single ended LVPECL, LVCMOS or LVTTL. A single enable pin is available to control both inputs. The SDI input pins are controlled by LVCMOS or LVTTL level signals. The NB6L295M 16 mA CML output contains temperature compensation circuitry. This device is offered in a 4 mm x 4 mm 24−pin QFN Pb−free package. The NB6L295M is a member of the ECLinPS MAX™ family of high performance products.

Features

- Input Clock Frequency > 1.5 GHz with 210 mV V_{OUTPP}
- Input Data Rate > 2.5 Gb/s
- Programmable Delay Range: 0 ns to 6 ns per Delay Channel
- Programmable Delay Range: 0 ns to 11.2 ns for EDb/s

Table 2. ATTRIBUTES

Characteristics		Value
Input Default State Resistors		37 kΩ
ESD Protection	Human Body Model Machine Model	> 2 kV > 100V
Moisture Sensitivity (Note 3)	QFN−24	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		3094
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}, V_{CC0}, V_{CC1}	Positive Power Supply	GND = 0 V		4.0	V
V_{IO}	Positive Input/Output Voltage	GND = 0 V	−0.5		

Table 4. DC CHARACTERISTICS, MULTI−LEVEL INPUTS V_{CC} = V_{CC0} = V_{CC1} = 2.375 V to 3.6 V, GND = 0 V, T_A = −40°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit
POWER SUPPLY CURRENT					
I_{CC}	Power Supply Current (Inputs, V_{TX} and Outputs Open) (Sum of I_{CC}, I_{CC0}, and I_{CC1})		170	215	mA
CML OUTPUTS (Notes 5 and 6, Figure 22)					
V_{OH}	Output HIGH Voltage V_{CC} = V_{CC0} = V_{CC1} = 3.3 V V_{CC} = V_{CC0} = V_{CC1} = 2.5 V	V_{CC} − 40 3260 2460	V_{CC} − 10 3290 2490	V_{CC} 3300 2500	mV
V_{OL}	Output LOW Voltage V_{CC} = V_{CC0} = V_{CC1} = 3.3 V V_{CC} = V_{CC0} = V_{CC1} = 2.5 V				

Serial Data Interface Programming

The NB6L295M is programmed by loading the 11−Bit SHIFT REGISTER using the SCLK, SDATA and SLOAD inputs. The 11 SDATA bits are 1 PSEL bit, 1 MSEL bit and 9 delay value data bitsD[8:0]. A separate 11−bit load cycle is required to program the delay data value of each channel, PD0 and PD1. For example, at powerup two load cycles will be needed to initially set PD0 and PD1; Dual Mode Operation as shown in Figures 3 and 4 and Extended Mode Operation as shown in Figures 5 and 6.

DUAL MODE OPERATIONS

PD0 Programmable Delay								Control Bits	
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1		Value

PD1 Programmable Delay	Control Bits	
		Value

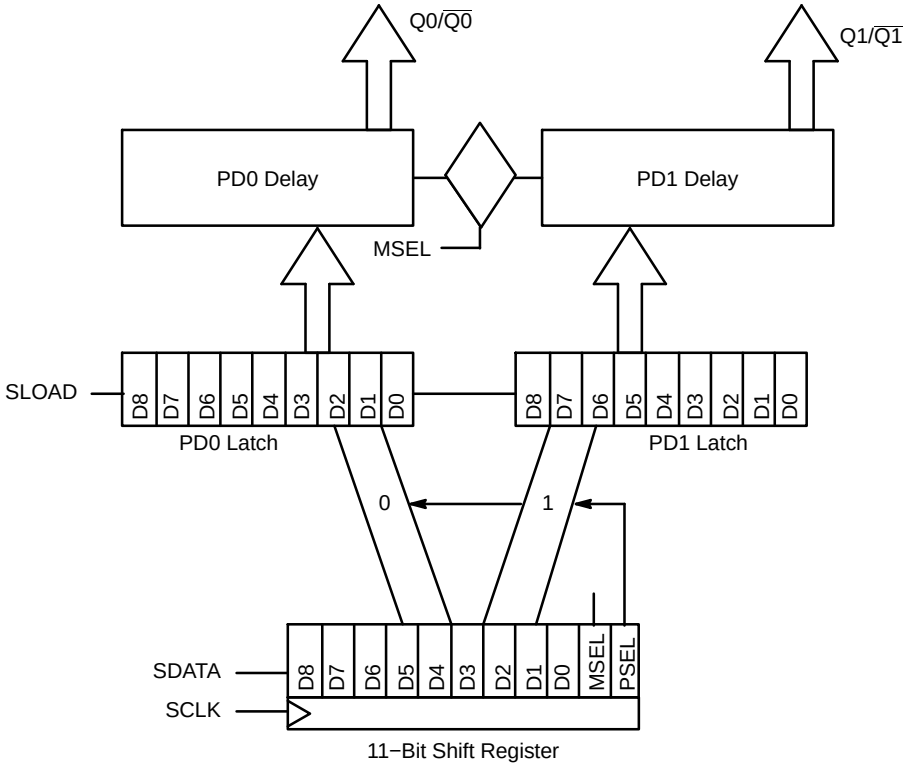


Figure 7. Serial Data Interface, Shift Register, Data Latch, Programmable Delay Channels Load Cycle Required for Each Channel

Serial Data Interface Loading

Loading the device through the 3 input Serial Data Interface (SDI) is accomplished by sending data into the SDIN pin by using the SCLK input pin and latching the data with the SLOAD input pin. The 11−bit SHIFT REGISTER shifts once per rising edge of the **SCLK** input. The serial input **SDIN** must meet setup and hold timing as specified in the AC Characteristics section of this document for each bit and clock pulse. The **SLOAD** line loads the value of the shift register on a LOW−to−HIGH edge transition (transparent state) into a data Latch register and latches the data with a subsequent HIGH−to−LOW edge transition. Further changes in SDIN or SCLK are not recognized by the latched register. The internal multiplexer states are set by the PSEL and MSEL bits in the SHIFT register. Figure 6 shows the timing diagram of a typical load sequence.

Input $\overline{EN}$ should be LOW (enabled) prior to SDI programming, then pulled HIGH (disabled) during programming. After programming, the $\overline{EN}$ should be returned LOW (enabled) for functional delay operation.

The disabling of $\overline{EN}$ (HIGH) forces Qx LOW and $\overline{Qx}$ HIGH and is included during programming to prevent (or mask out) any potential run pulses or extended pulses which might occur in the internal delay gates programming switching, but it is not required for programming.

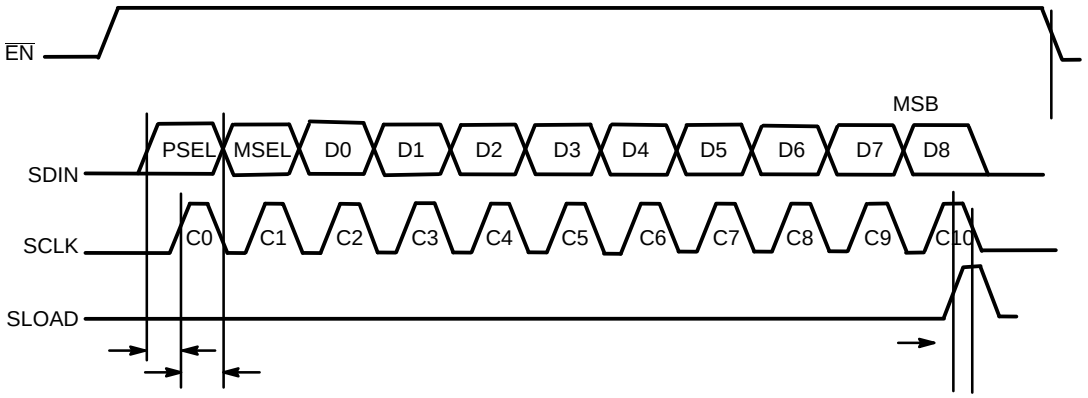


Figure 8. SDI Programming Cycle Timing Diagram (Load Cycle 1 of 2)

Table 7 shows theoretical values of delay capabilities in both the Dual Delay Mode and in the Extended Delay Modes of operation.

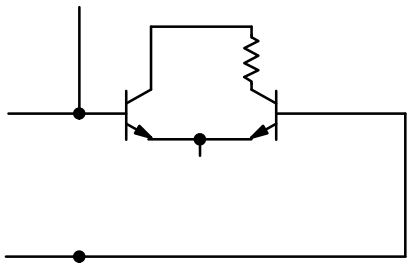


Figure 9. Input Structure

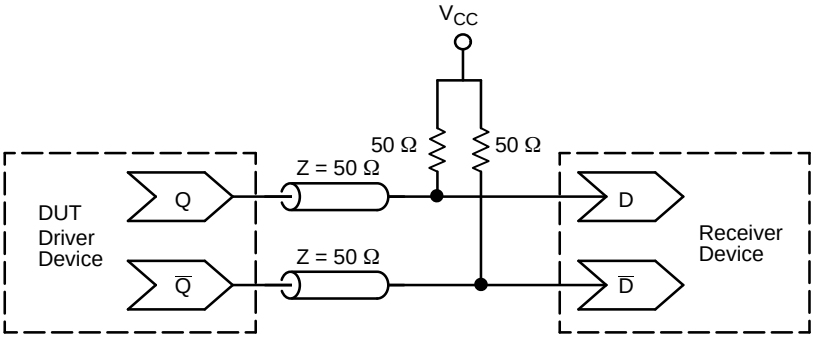


Figure 22. Typical Termination for Output Driver and Device Evaluation

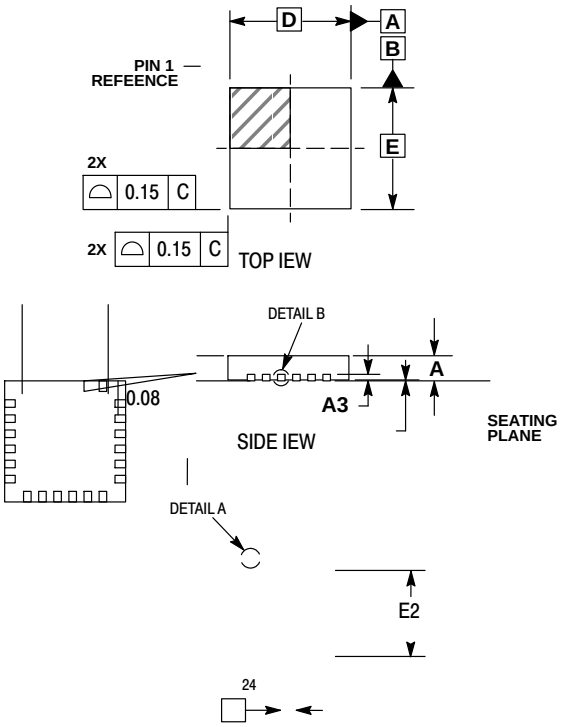
Figure 23. Output Voltage Amplitude (V_{OUTPP}) vs. Output Frequency at Ambient Temperature (Typical)

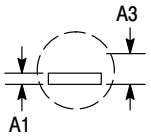
QFN24, 4x4, 0.5P
CASE 485L
ISSUE B

DATE 05 JUN 2012

f2.8246041 cm 0 0

SCALE 2:1





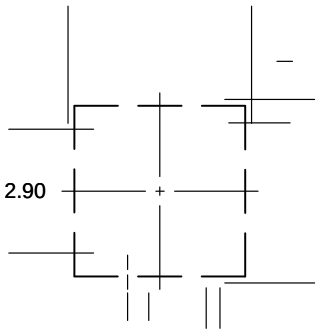
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

GENERIC
MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS