

performance products.

Feat

- In Hz with 550 mV
- In
- Pr ns to 6 ns per Delay
- Cl
- Pr ns to 11.2 ns for
- Ex
- To 8 ns per Delay Channel
- To ns in Extended Delay
- M
- M nents in 511 Steps
- Li
- 10 mes

- 3 ps Typical Clock Jitter, RMS
- 20 ps Pk-Pk Typical Data Dependent Jitter
- LVPECL, CML or LVDS Differential Input Compatible
- LVPECL, LVCMOS, LVTTTL Single-Ended Input Compatible
- 3-Wire Serial Interface
- Input Enable/Disable
- Operating Range: $V_{CC} = 2.375\text{ V to }3.6\text{ V}$
- LVPECL Output Level; 780 mV Peak-to-Peak, Typical
- Internal $50\ \Omega$ Input Termination Provided
- $-40^{\circ}\text{C to }85^{\circ}\text{C}$ Ambient Operating Temperature
- 24-Pin QFN, 4 mm x 4 mm
-

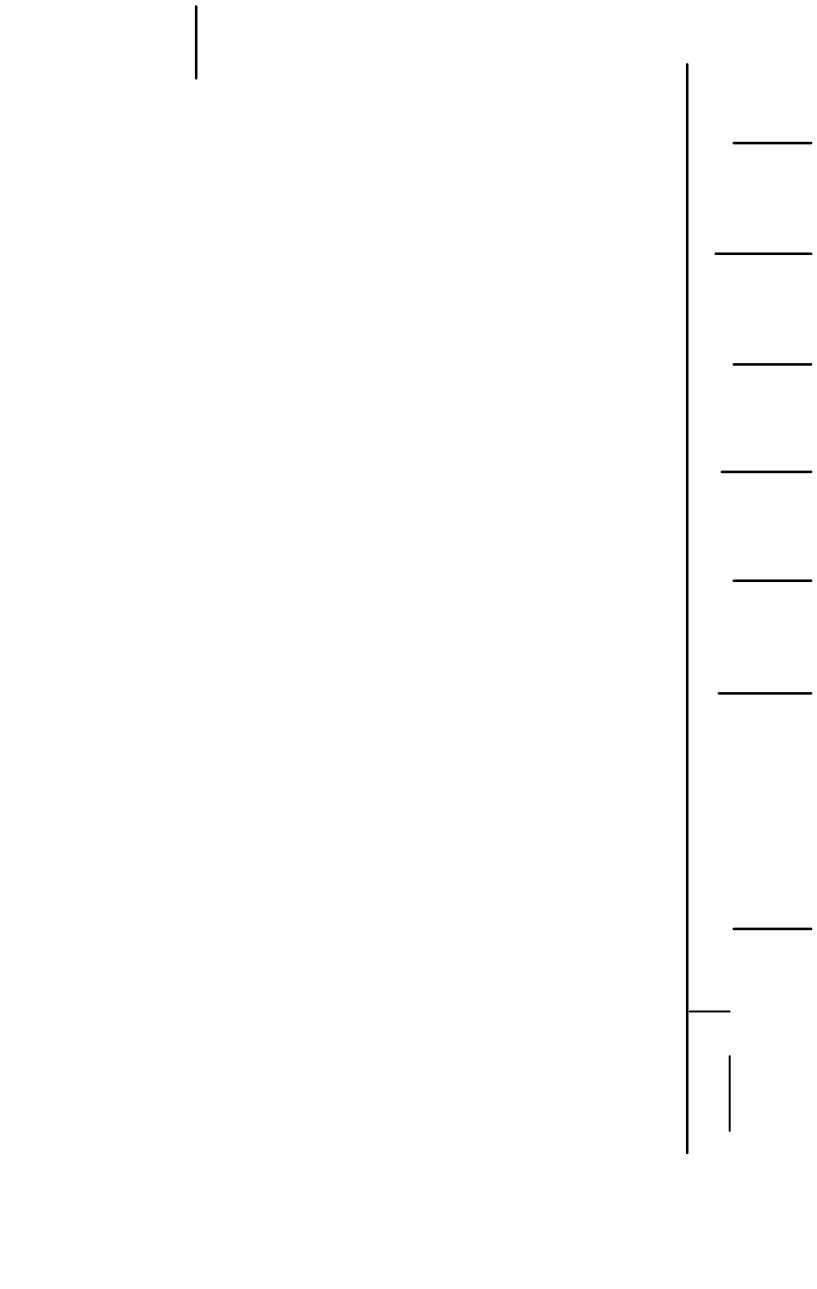
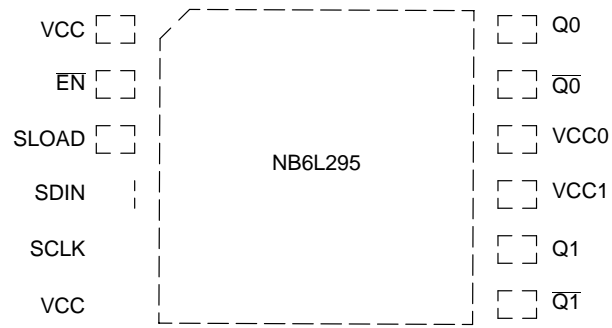


Figure 1. Simplified Functional Block Diagram

NB6L295

VT0 IN0 $\overline{IN0}$ $\overline{VT0}$ GND VCC0



VT1 IN1 $\overline{IN1}$ $\overline{VT1}$ GND VCC1

NB6L295

Table 2. ATTRIBUTES

| Characteristics | Value |
|-------------------------------|------------------|
| Input Default State Resistors | 37 kΩ |
| ESD Protection | Human Body Model |

NB6L295

Table 4. DC CHARACTERISTICS, MULTI-LEVEL INPUTS $V_{CC} = V_{CC0} = V_{CC1} = 2.375\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$

| Symbol | Characteristic | Min | Typ | Max | Unit |
|--------|----------------|-----|-----|-----|------|
|--------|----------------|-----|-----|-----|------|

POWER SUPPLY CURRENT

| | | | | | |
|----------|---|-----|-----|-----|----|
| I_{CC} | Power Supply Current (Inputs, V_{TX} and Outputs Open) (Sum of I_{CC} , I_{CC0} , and I_{CC1}) | 110 | 140 | 170 | mA |
|----------|---|-----|-----|-----|----|

LVPECL OUTPUTS (Notes 5 and 6, Figure 21)

| | | | | | |
|----------|---|---------------------------------|--------------------------------|--------------------------------|----|
| V_{OH} | Output HIGH Voltage $V_{CC} = V_{CC0} = V_{CC1} = 3.3\text{ V}$ $V_{CC} = V_{CC0} = V_{CC1} = 2.5\text{ V}$ | $V_{CC} - 1075$ 2225 1425 | $V_{CC} - 950$ 2350 1550 | $V_{CC} - 825$ 2475 1675 | mV |
| V_{OL} | Output LOW Voltage $V_{CC} = V_{CC0} = V_{CC1} = 3.3\text{ V}$ $V_{CC} = V_{CC0} = V_{CC1} = 2.5\text{ V}$ | $V_{CC} - 1825$ 1475 | $V_{CC} - 1725$ 1575 | $V_{CC} - 1625$ 1675 | mV |
| | | $V_{CC} - 1825$ 675 | $V_{CC} - 1725$ 775 | $V_{CC} - 1600$ 900 | |

DIFFERENTIAL INPUT DRIVEN SINGLE-ENDED (see Figures 10 and 11) (Note 7)

| | | | | | |
|-----------|--|----------------|--|----------------|----|
| V_{th} | Input Threshold Reference Voltage Range | 1050 | | $V_{CC} - 150$ | mV |
| V_{IH} | Single-Ended Input HIGH Voltage | $V_{th} + 150$ | | V_{CC} | mV |
| V_{IL} | Single-Ended Input LOW Voltage | GND | | $V_{th} - 150$ | mV |
| V_{ISE} | Single-Ended Input Voltage Amplitude ($V_{IH} - V_{IL}$) | 300 | | $V_{CC} - GND$ | mV |

DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (see Figures 12 and 13) (Note 8)

| | | | | | |
|-----------|--|------|--|----------------|---------------|
| V_{IHD} | Differential Input HIGH Voltage | 1200 | | V_{CC} | mV |
| V_{ILD} | Differential Input LOW Voltage | GND | | $V_{CC} - 150$ | mV |
| V_{ID} | Differential Input Voltage Swing ($I_{NX}, \overline{I_{NX}}$) ($V_{IHD} - V_{ILD}$) | 150 | | $V_{CC} - GND$ | mV |
| V_{CMR} | Input Common Mode Range (Differential Configuration) (Note 9) | 950 | | $V_{CC} - 75$ | mV |
| I_{IH} | Input HIGH Current $I_{NX}/\overline{I_{NX}}$, ($V_{Tn}/\overline{V_{Tn}}$ Open) | -150 | | 150 | μA |
| I_{IL} | Input LOW Current $I_{NX}/\overline{I_{NX}}$, ($V_{Tn}/\overline{V_{Tn}}$ Open) | -150 | | 150 | μA |

SINGLE-ENDED LVCMOS/LVTTL CONTROL INPUTS

| | | | | | |
|----------|---------------------------------|------|--|----------|---------------|
| V_{IH} | Single-Ended Input HIGH Voltage | 2000 | | V_{CC} | mV |
| V_{IL} | Single-Ended Input LOW Voltage | GND | | 800 | mV |
| I_{IH} | Input HIGH Current | -150 | | 150 | μA |
| I_{IL} | Input LOW Current | -150 | | 150 | μA |

TERMINATION RESISTORS

| | | | | | |
|-----------|-------------------------------------|----|----|----|----------|
| R_{TIN} | Internal Input Termination Resistor | 40 | 50 | 60 | Ω |
|-----------|-------------------------------------|----|----|----|----------|

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printe-150V

NB6L295

Table 5. AC CHARACTERISTICS $V_{CC} = V_{CC0} = V_{CC1} = 2.375 \text{ V to } 3.6 \text{ V}$, $GND = 0 \text{ V}$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ (Note 10)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|-------------|---|-----|--------|--|------|
| f_{SCLK} | Serial Clock Input Frequency, 50% Duty Cycle | | | 20 | MHz |
| V_{OUTPP} | Output Voltage Amplitude (@ $V_{INPPmin}$) $f_{in} \leq 1.5 \text{ GHz}$ (Note 15) (See Figure 22) | 530 | 780 | | mV |
| f_{DATA} | Maximum Data Rate (Note 14) | 2.5 | | | Gb/s |
| t_{Range} | Programmable Delay Range (@ 50 MHz) Dual Mode $IN0/\overline{IN0}$ to $Q0/\overline{Q0}$ or $IN1/\overline{IN1}$ to $Q1/\overline{Q1}$ Extended Mode $IN0/\overline{IN0}$ to $Q1/\overline{Q1}$ | 0 | 5.7 | | |
| | | 0 | 104 uJ | TJET376.214 78 262.2047 6.1 .9071 refBT8 0 0 8 1 | |

Serial Data Interface Programming

NB6L295



NB6L295

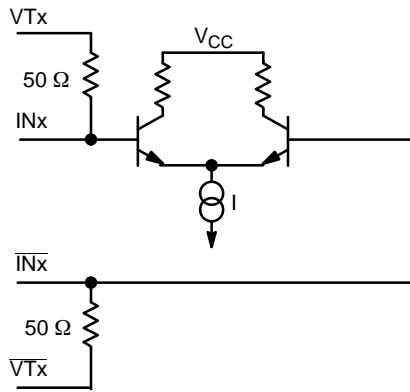


Figure 9. Input Structure

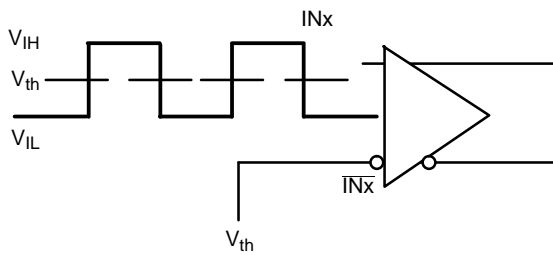


Figure 10. Differential Input Driven Single-Ended

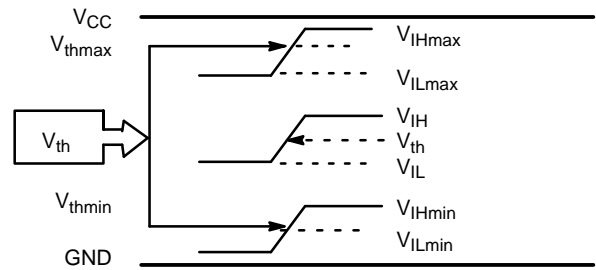


Figure 11. V_{th} Diagram

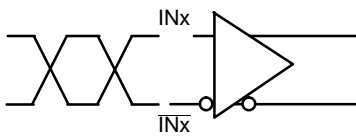
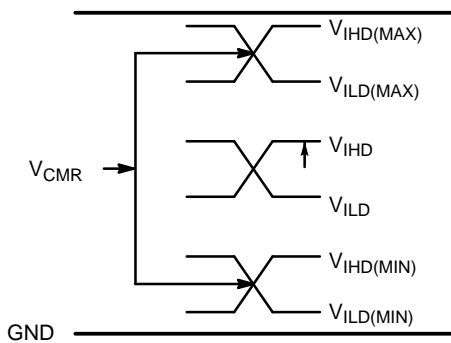


Figure 12. Differential Inputs Driven Differentially



NB6L295

NB6L295

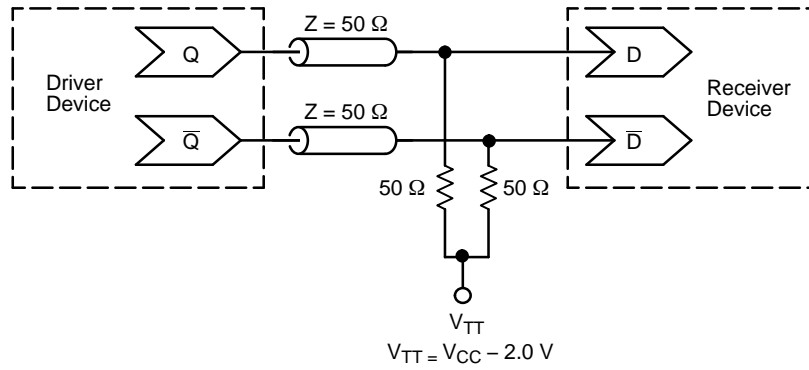


Figure 21. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

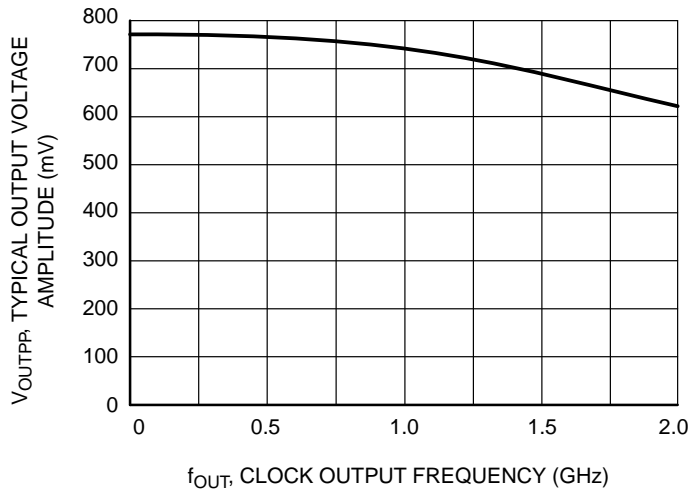


Figure 22. Output Voltage Amplitude (V_{OUTPP}) vs. Output Frequency at Ambient Temperature (Typical)

ORDERING INFORMATION

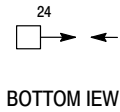
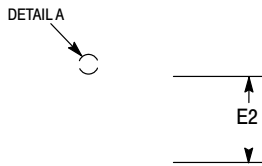
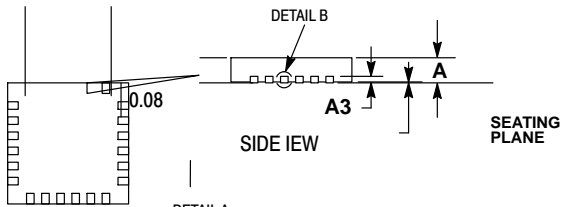
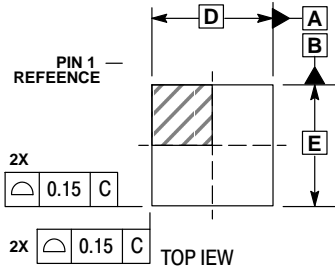
| Device | Package | Shipping [†] |
|------------|---------------------|-----------------------|
| NB6L295MNG | QFN-24 (Pb-free) | 92 Units / Rail |

NB6L295MNTXef59.754 288.5uC1 6.5 -6.5 0 167/ Rt37u6.23s5m6.5 0-11CY (GHz Tm(+))Tj o2759.754 288.51 155.395 .68033 refBT8358.639 71.559 279

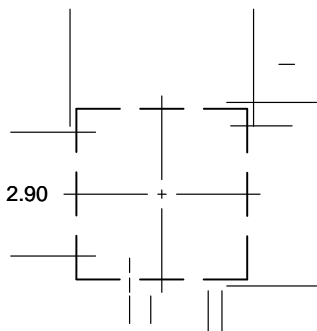
QFN24, 4x4, 0.5P
CASE 485L
ISSUE B

DATE 05 JUN 2012

f2.826041 cm 0 0
SCALE 2:1



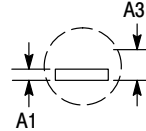
SOLDERING FOOTPRINT



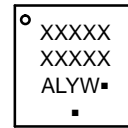
DIMENSIONS: MILLIMETERS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

onsemi, **onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi**
