# 3.3 V 100/133 MHz Differential 1:8 HCSL-Compatible Push-Pull Clock ZDB/Fanout Buffer for PCIe®

# NB3W800L

### Description

The NB3W800L is a low−power 8−output differential buffer that meets all the performance requirements of the DB800ZL specification. The NB3W800L is capable of distributing the reference clocks for Intel® QuickPath Interconnect (Intel QPI and UPI), PCIe Gen1/Gen2/Gen3/Gen4, SAS, SATA, and Intel Scalable Memory Interconnect (Intel SMI) applications. A fixed, internal feedback path maintains low drift for critical QPI applications.

### Features

- 8 Differential Clock Output Pairs @ 0.7 V
- Low−power NMOS Push−pull HCSL Compatible Outputs
- Cycle−to−cycle Jitter <50 ps
- Output−to−output Skew <50 ps
- Input−to−output Delay Variation <100 ps
- PCIe Phase Jitter: Gen3 <1.0 ps, Gen4 <0.5 ps RMS
- QPI 9.6GT/s 12UI Phase Jitter <0.2 ps RMS
- Pseudo−External Fixed Feedback for Lowest Input−to−Output Delay
- Individual OE Control; Hardware Control of Each Output
-

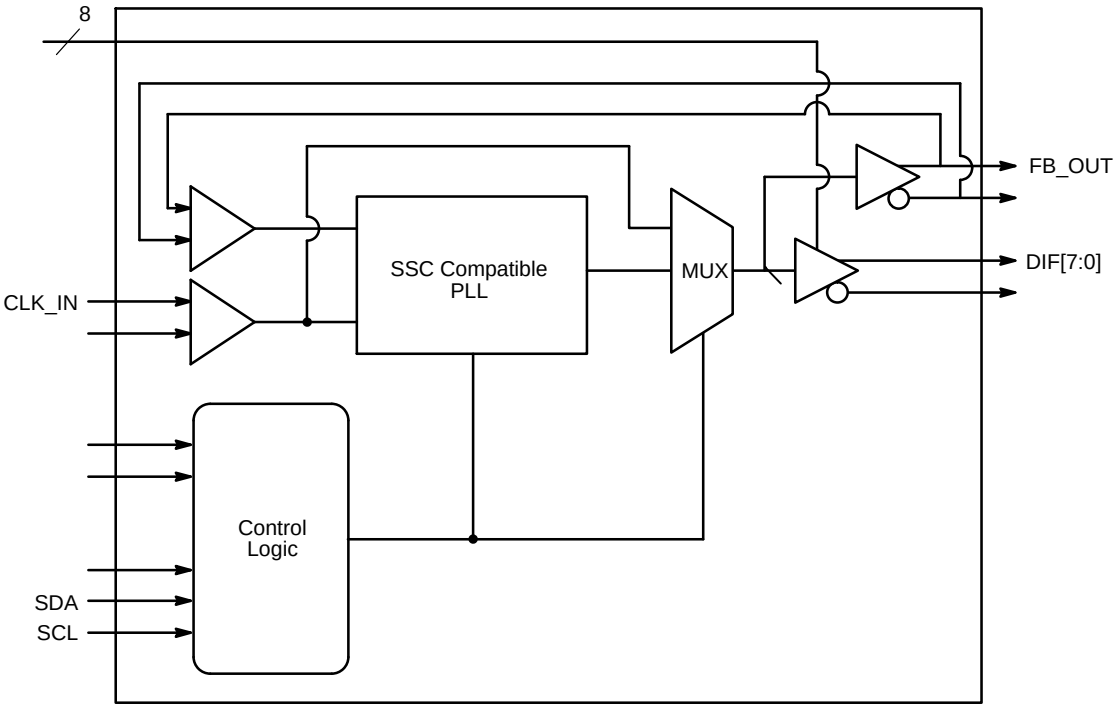


**Figure 1. Simplified Block Diagram**

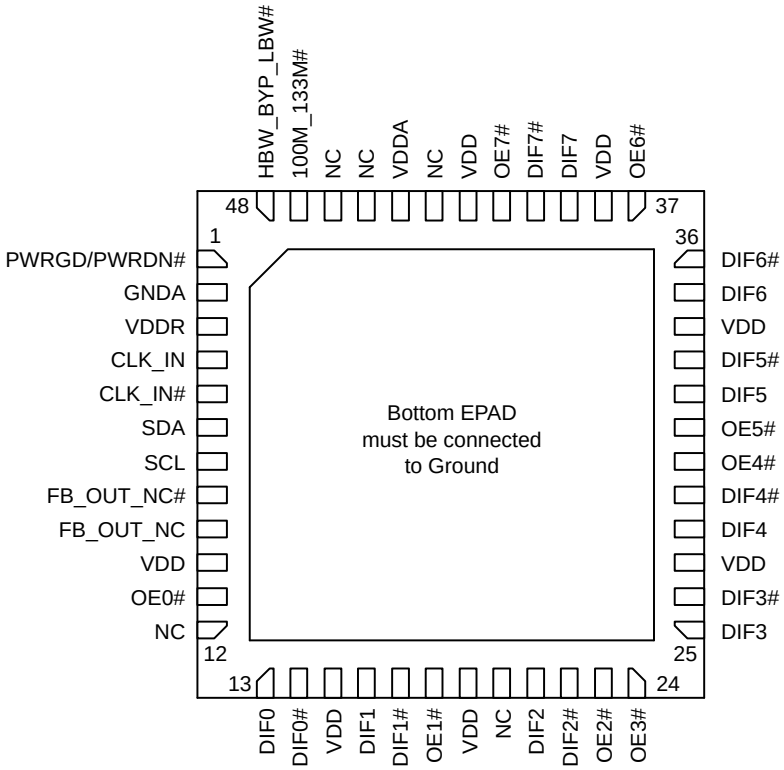


**Figure 2. Pin Configuration**

**Table 8. PIN DESCRIPTIONS**

| Pin # | Pin Name | Type | Description |
|---|---|---|---|
| 1 | PWRGD/PWRDN# | IN | 3.3 V Input notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode. |
| 2 | GNDA | GND | Ground for Input Receiver and PLL Core |
| 3 | VDDR | PWR | 3.3 V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. |
| 4 | CLK_IN | IN | 0.7 V Differential true input |
| 5 | CLK_IN# | IN | 0.7 V Differential complementary Input |
| 6 | SDA | I/O | Data pin of SMBus circuitry |
| 7 | | | |

**Table 8. PIN DESCRIPTIONS**

| Pin # | Pin Name | Type | Description |
|---|---|---|---|
| 17 | DIF1# | OUT | 0.7 V differential complementary clock output |
| 18 | OE1# | IN | Active low input for enabling DIF pair 1. This pin has an internal pull down. 1 =disable outputs, 0 = enable outputs |
| 19 | VDD | PWR | Power supply, nominal 3.3 V |
| 20 | NC | N/A | No Connection. |
| 21 | DIF2 | OUT | 0.7 V differential true clock output |
| 22 | DIF2# | OUT | 0.7 V differential complementary clock output |
| 23 | OE2# | IN | Active low input for enabling DIF pair 2. This pin has an internal pull down. 1 = disable outputs, 0 = enable outputs |
| 24 | OE3# | IN | Active low input for enabling DIF pair 3. This pin has an internal pull down. 1 = disable outputs, 0 = enable outputs |
| 25 | DIF3 | OUT | 0.7 V differential true clock output |
| 26 | DIF3# | OUT | 0.7 V differential complementary clock output |
| 27 | VDD | PWR | Power supply, nominal 3.3 V |
| 28 | DIF4 | OUT | 0.7 V differential true clock output |
| 29 | DIF4# | OUT | 0.7 V differential complementary clock output |
| 30 | OE4# | IN | Active low input for enabling DIF pair 4. This pin has an internal pull down. 1 = disable outputs, 0 = enable outputs |
| 31 | OE5# | IN | Active low input for enabling DIF pair 5. This pin has an internal pull down. 1 =disable outputs, 0 = enable outputs |
| 32 | DIF5 | OUT | 0.7 V differential true clock output |
| 33 | DIF5# | OUT | 0.7 V differential complementary clock output |
| 34 | VDD | PWR | Power supply, nominal 3.3 V |
| 35 | DIF6 | OUT | 0.7 V differential true clock output |
| 36 | DIF6# | OUT | 0.7 V differential complementary clock output |
| 37 | OE6# | IN | Active low input for enabling DIF pair 6. This pin has an internal pull down. 1 = disable outputs, 0 = enable outputs |
| 38 | VDD | PWR | Power supply, nominal 3.3 V |
| 39 | DIF7 | OUT | 0.7 V differential true clock output |
| 40 | DIF7# | OUT | 0.7 V differential complementary clock output |
| 41 | OE7# | IN | Active low input for enabling DIF pair 7. This pin has an internal pull down. 1 = disable outputs, 0 = enable outputs |
| 42 | VDD | PWR | Power supply, nominal 3.3 V |
| 43 | NC | N/A | No Connection. |
| 44 | VDDA | PWR | 3.3 V power for the PLL core. |
| 45 | NC | N/A | No Connection. |
| 46 | NC | N/A | No Connection. |
| 47 | 100M_133M# | IN | 3.3 V Input to select operating frequency. See Functionality Table for Definition |
| 48 | HBW_BYP_LBW# | IN | Trilevel input to select High BW, Bypass or Low BW mode. See PLL Operating Mode Table for Details. |
| 49 | GND | PWR | EPAD, must be connected to Ground |

**Table 9. ABSOLUTE MAXIMUM RATINGS**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| VDD, VDDA | 3.3 V Supply Voltage (Notes 1, 2) | VDD for core logic and PLL | | | 4.6 | V |
| $V_{IL}$ | Input Low Voltage (Note 1) | | GND 0.5 | | | V |
| $V_{IH}$ | Input High Voltage (Note 1) | Except for SMBus interface | | | $V_{DD}$ + 0.5 | V |
| $V_{IHSMB}$ | Input High Voltage (Note 1) | SMBus clock and data pins | | | 5.5 | V |

**Table 12. DIF 0.7 V AC TIMING CHARACTERISTICS (Non−Spread or −0.5% Spread Spectrum Mode)**
($V_{DD}$ = $V_{DDA}$ = 3.3 V ±5%, $T_A$ = 0°C − 70°C), See Test Loads for Loading Conditions.

| Symbol | Parameter | | CLK = 100 MHz, 133.33 MHz | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Tstab (Note 32) | Clock Stabilization Time | | | 1.8 | ms |
| Laccuracy (Notes 15, 19, 27, 33) | Long Accuracy | | | 100 | ppm |
| Tabs (Notes 15, 16, 19) | Absolute Min/Max Host CLK Period | No Spread | 9.94900 for 100 MHz | 10.05100 for 100 MHz | ns |
| | | | 7.44925 for 133 MHz | 7.55075 for 133 MHz | |
| | | 0.5% Spread | 9.49900 for 100 MHz | 10.10126 for 100 MHz | |
| | | | 7.44925 for 133 MHz | 7.58845 for 133 MHz | |
| Slew_rate (Notes 13, 15, 19) | DIFF OUT Slew_rate | | 1.0 | 4.0 | V/ns |
| ΔTrise / ΔTfall (Notes 15, 19, 29) | Rise and Fall Time Variation | | | 125 | ps |
| Rise/Fall Matching (Notes 15, 19, 30, 31) | | | | 20 | % |
| VHigh (Notes 15, 18, 21) | Voltage High (typ 0.70 Volts) | | 660 | 850 | mV |
| VLow (Notes 15, 18, 22) | | | | | |

**Table 13. ELECTRICAL CHARACTERISTICS – Current Consumption**
($V_{DD}$ = V

**Table 15. ELECTRICAL CHARACTERISTICS – PHASE JITTER PARAMETERS**
($V_{DD}$ = $V_{DDA}$ = 3.3 V ±5%, TA = 0°C  70°C), See Test Loads for Loading Conditions. (Note 35)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{jphPCIeG1}$ | Phase Jitter, PLL Mode (Note 47) | PCIe Gen 1 (Notes 48, 49) | | 13 | 86 | ps (p  p) |
| $t_{jphPCIeG2}$ | | PCIe Gen 2 Lo Band 10 kHz < f < 1.5 MHz (Note 48) | | 0.25 | 3.0 | ps (rms) |
| | | PCIe Gen 2 High Band 1.5 MHz < f < Nyquist (50 MHz) (Note 48) | | 1.05 | 3.1 | ps (rms) |
| $t_{jphPCIeG3}$ | | PCIe Gen 3 (PLL BW of 2  4 MHz, CDR = 10 MHz) (Notes 48, 50) | | 0.21 | 1.0 | ps (rms) |
| $t_{jphPCIeG4}$ | | PCIe Gen 4 (PLL BW of 2  4 MHz, CDR = 10 MHz) (Notes 48, 50) | | 0.21 | 0.5 | ps (rms) |
| $t_{jphUPI}$ | | UPI (9.6 Gb/s, 10.4 Gb/s or 11.2 Gb/s, 100 MHz, 12 UI) | | 0.7 | 1.0 | ps (rms) |
| $t_{jphQPI\_SMI}$ | | QPI & SMI (100 MHz or 133 MHz, 4.8 Gb/s, 6.4 Gb/s 12 UI) (Note 51) | | 0.14 | 0.5 | ps (rms) |
| | | QPI & SMI (100 MHz, 8.0 Gb/s, 12 UI) (Note 51) | | 0.1 | 0.3 | ps (rms) |
| | | QPI & SMI (100 MHz, 9.6 Gb/s, 12 UI) (Note 51) | | 0.08 | 0.2 | ps (rms) |
| $t_{jphPCIeG1}$ | Additive Phase Jitter, Bypass mode (Note 47) | PCIe Gen 1 (Notes 48, 49) | | | 10 | ps (p  p) |
| $t_{jphPCIeG2}$ | | PCIe Gen 2 Lo Band 10 kHz < f < 1.5 MHz (Notes 48, 52) | | | 0.3 | ps (rms) |
| | | PCIe Gen 2 High Band 1.5 MHz < f < Nyquist (50 MHz) (Notes 48, 52) | | | 0.6 | ps (rms) |
| $t_{jphPCIeG3}$ | | PCIe Gen 3 (PLL BW of 2  4 MHz, 2  5 MHz, CDR = 10 MHz) (Notes 48, 50, 52) | | | 0.2 | ps (rms) |
| $t_{jphQPI\_SMI}$ | | QPI & SMI (100 MHz or 133 MHz, 4.8 Gb/s, 6.4 Gb/s 12 UI) (Notes 51, 52) | | | 0.2 | ps (rms) |
| | | QPI & SMI (100 MHz, 8.0 Gb/s, 12 UI) (Notes 51, 52) | | | 0.1 | ps (rms) |
| | | QPI & SMI (100 MHz, 9.6 Gb/s, 12 UI) (Notes 51, 52) | | | 0.1 | ps (rms) |

47. Applies to all outputs.
48. See http://www.pcisig.com for complete specs
49. Sample size of at least 100K cycles. This figures extrapolates to 108ps pk  pk @ 1M cycles for a BER of 1  12.
50. Subject to final ratification by PCI SIG.
51. Calculated from Intel  supplied Clock Jitter Tool v 1.6.3
52. For RMS figures, additive jitter is calculated by solving the following equation: (Additive jitter)$^2$ = (total jittter)$^2$ - (input jitter)$^2$

**Table 16. CLOCK PERIODS – Differential Outputs with Spread Spectrum Disabled**

| | | Measurement Window | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 1 Clock | 1 μs | 0.1 s | 0.1 s | 0.1 s | 1 μs | 1 Clock | |
| SSC OFF | Center Freq. MHz | −c2c Jitter Abs Per Min | −SSC Short−Term Average Min | − ppm Long−Term Average Min | 0 ppm Period Nominal | + ppm Long−Term Average Max | +SSC Short−Term Average Max | +c2c Jitter Abs Per Max | Units |
| DIF | | | | | | | | | |

## MEASUREMENT POINTS FOR DIFFERENTIAL

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## SIGNAL AND FEATURE OPERATION

### CLK_IN, CLK_IN#

The differential input clock is expected to be sourced from a clock synthesizer with an HCSL−compatible output, e.g. CK420BQ, CK−NET, CK−uS, or CK509B or another driver.

### OE# and Output Enables (Control Registers)

Each output can be individually enabled or disabled by SMBus control register bits. Additionally, each output of the DIF[7:0] has a dedicated OE# pin. The OE# pins are asynchronous asserted−low signals. The Output Enable bits in the SMBus registers are active high and are set to enable by default.

The disabled state for the NB3W800L low power NMOS Push−Pull outputs is Low/Low.

Please note that the logic level for assertion or deassertion is different in software than it is on hardware. Output is enabled if OE# pin is pulled low and still maintains software programming logic with output enabled if OE register is true.

The assertion and de−assertion of this signal is absolutely asynchronous.

### OE# Assertion (Transition from ‘1’ to ‘0’)

All differential outputs that were tristated will resume normal operation in a glitch free manner.

### OE# De−Assertion (Transition from ‘0’ to ‘1’)

Corresponding output will transition from normal operation to tri−state in a glitch free manner.

### 100M_133M# − Frequency Selection

The 100M_133M# is a hardware pin, which programs the appropriate output frequency of the DIF pairs. Note that the CLK_IN frequency is equal to CLK_OUT frequency. An external pull−up or pull−down resistor is attached to this pin to select the input/output frequency.

### PWRGD/PWRDN#

PWRGD/PWRDN# is a dual function pin. PWRGD is asserted high and de−asserted low. De−assertion of PWRGD (pulling the signal low) is equivalent to indicating a powerdown condition. PWRGD (assertion) is used by the NB3W800L to sample initial configurations such as frequency select condition and SA selections.

After PWRGD has been asserted high for the first time, the pin becomes a PWRDN# (Power Down) pin that can be used to shut off all clocks cleanly and instruct the device to invoke power savings mode. PWRDN# is a completely asynchronous active low input. When entering power savings mode, PWRDN# should be asserted low **prior to shutting off the input clock or power** to ensure all clocks shut down in a glitch free manner. When PWRDN# is asserted low by two consecutive rising edges of DIF#, all differential outputs are held tri−stated on the next DIF# high to low transition. The assertion and de-assertion of PWRDN# is absolutely asynchronous.

**WARNING:** Disabling of the CLK_IN input clock prior to assertion of PWRDN# is an undefined mode and not recommended. Operation in this mode may result in glitches, excessive frequency shifting, etc.

**Table 18. PWRGD/PWRDN# FUNCTIONALITY**

| PWRGD/PWRDN# | DIF | DIF# |
|---|---|---|
| 0 | Tri state | Tri state |
| 1 | Running | Running |

### HBW_BYPASS_LBW#

The HBW_BYPASS_LBW# is a tri level function input pin. It is used to select between PLL high bandwidth, bypass mode and PLL low bandwidth mode.

## POWER FILTERING EXAMPLE

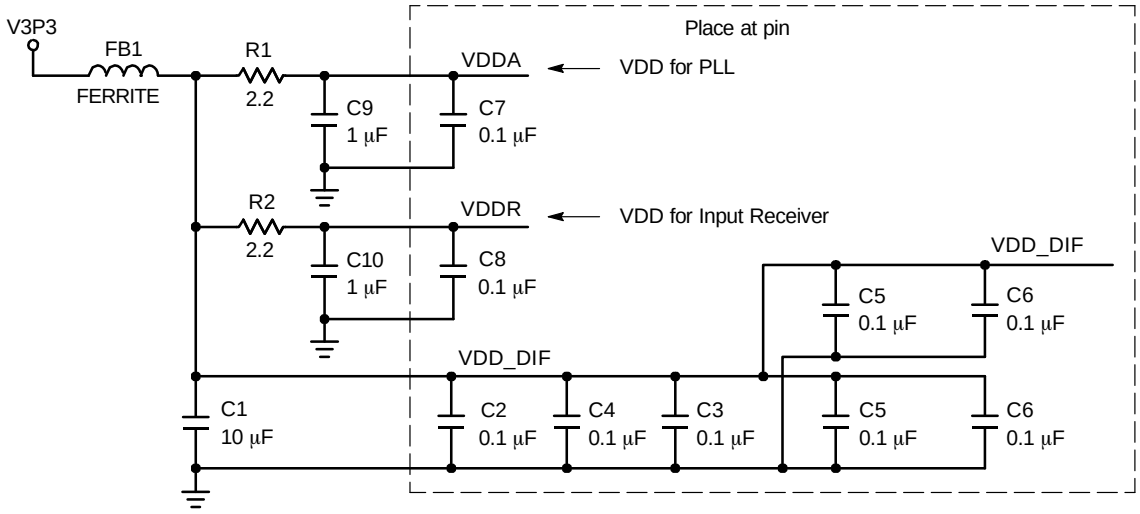


**Figure 7. Schematic Example of the NB3W800L Power Filtering**

### Buffer Power−Up State Machine

**Table 19. BUFFER POWER−UP STATE MACHINE**

| State | Description |
|---|---|
| 0 | 3.3 V Buffer power off |
| 1 | After 3.3 V supply is detected to rise above 3.135 V, the buffer enters State 1 and initiates a 0.1 ms–0.3 ms delay. |
| 2 | Buffer waits for a valid clock on the CLK input and PWRDN# de assertion (or PWRGD assertion low to high) |
| 3 | Once the PLL is locked to the CLK_IN input clock, the buffer enters state 3 and enables outputs for normal operation. (Notes 57, 58) |

57. The total power up latency from power on to all outputs active must be less than 1.8 ms (assuming a valid clock is present on CLK_IN input).
58. If power is valid and powerdown is de asserted (PWRGD asserted) but no input clocks are present on the CLK_IN input, DIF clocks must remain disabled. Only after valid input clocks are detected, valid power, PWRDN# de asserted (PWRGD asserted) with the PLL locked/stable and the DIF outputs enabled.

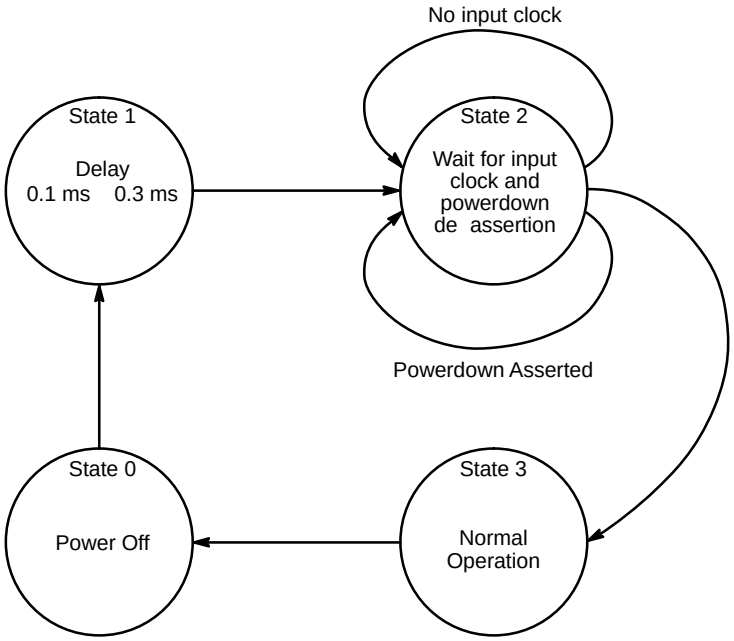


**Figure 8. Buffer Power−Up State Diagram**

### Device Power−Up Sequence

Follow the power−up sequence below for proper device functionality:

1. PWRGD/PWRDN# pin must be Low.
2. Assign remaining control pins to their required state (100M_133M#, HBW_BYPASS_LBW#, SDA, SCL)
3. Apply power to the device.
4. Once the VDD pin has reached a valid VDDmin level (3.3V −5%), the PWRGD/PWRDN# pin must be asserted High. See Figure 9.

Note: If no clock is present on the CLK_IN/CLK_IN# pins when device is powered up, there will be no clock on DIF/DIF# outputs.

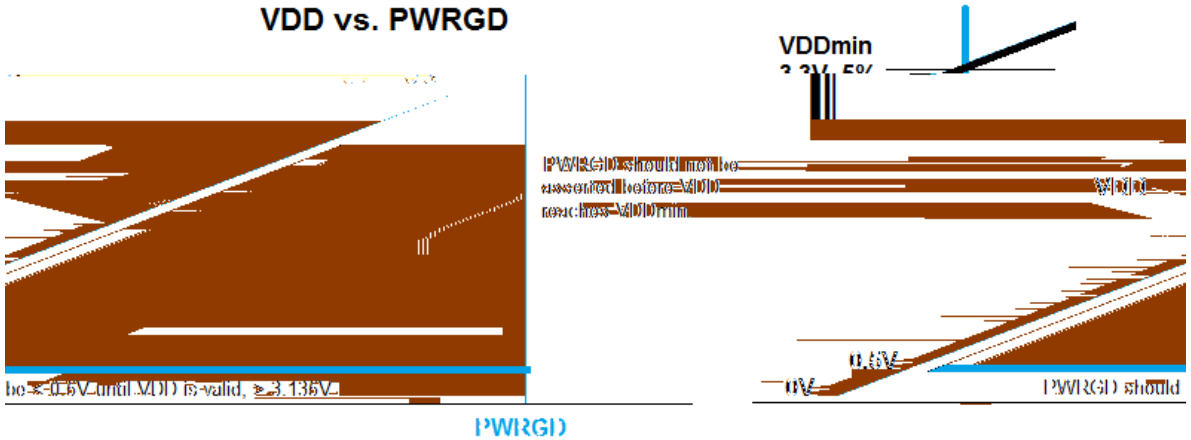


**Figure 9. PWRGD and VDD Relationship Diagram**

**Table 20. SMBus TABLE: PLL MODE, AND FREQUENCY SELECT REGISTER**

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| Bit 7 | 48 | PLL Mode 1 | PLL Operating Mode Rd back 1 | R | See PLL Operating Mode Readback Table | | |

**Table 24. SMBus TABLE: RESERVED REGISTER**

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| Bit 7 | | Reserved | | | | | 0 |
| Bit 6 | | Reserved | | | | | 0 |
| Bit 5 | | Reserved | | | | | 0 |
| Bit 4 | | Reserved | | | | | 0 |
| Bit 3 | | Reserved | | | | | 0 |
| Bit 2 | | Reserved | | | | | 0 |
| Bit 1 | | Reserved | | | | | 0 |
| Bit 0 | | Reserved | | | | | 0 |

**Table 25. SMBus TABLE: VENDOR & REVISION ID REGISTER**

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|---|
| Bit 7 | | | | | | | |

**QFN48 6x6, 0.4P**
CASE 485DP
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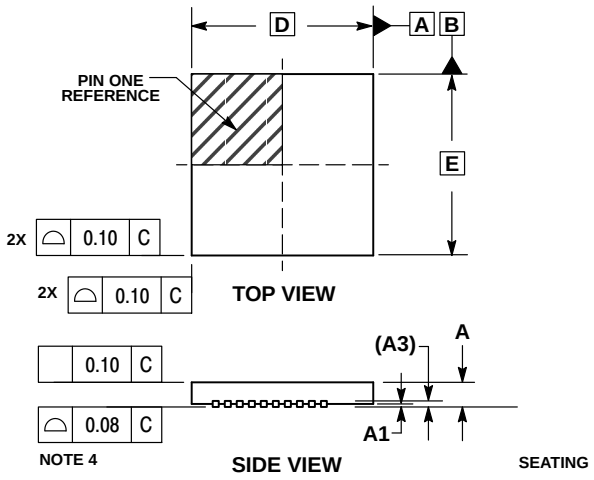
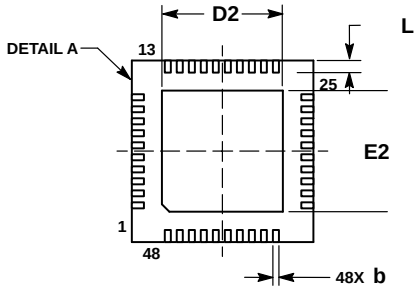
DATE 27 MAY 2014

**SCALE 2:1**




**BOTTOM VIEW**