The NB3N51054 is a precision, low phase noise clock generator that supports PCI Express requirements. The device accepts a 25 MHz fundamental mode parallel resonant crystal or a 25 MHz reference clock signal and generates four differential HCSL/LVDS outputs (See Figure 7 for LVDS interface) at 100 MHz clock frequency with maximum skew of 40 ps. Through I^2C interface, NB3N51054 provides selectable spread spectrum options of −0.35% and −0.5% for applications demanding low Electromagnetic Interface (EMI) as well as optimum performance with no spread option. The I^2C interface further enables control of each output and they can be enabled/disabled individually.

Features

- Uses 25 MHz Fundamental Crystal or Reference Clock Input
- Four Low Skew HCSL or LVDS Outputs
- I^2C Support with Read Back Capability
- [illegible] options of

BLOCK DIAGRAM

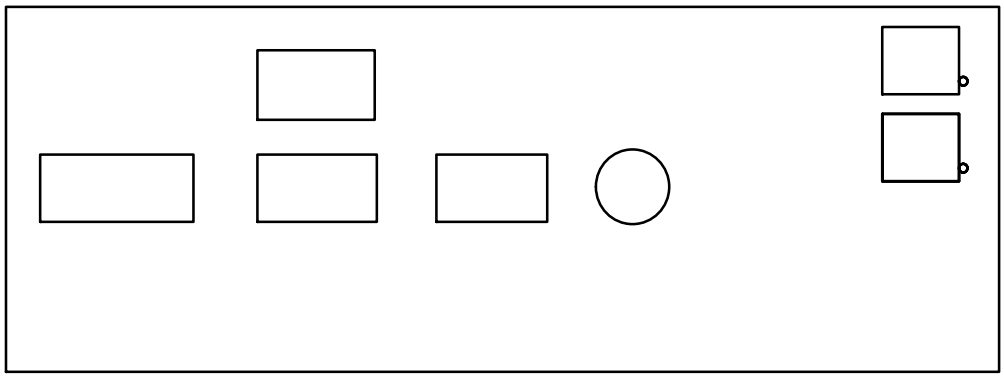


Table 1. PIN DESCRIPTION

Pin #	Pin Name	Type	Description

Recommended Crystal Parameters

Crystal	Fundamental AT−Cut
Frequency	25 MHz
Load Capacitance	16−20 pF
Shunt Capacitance, C0	7 pF Max
Equivalent Series Resistance	50 Max
Initial Accuracy at 25 °C	±20 ppm
Temperature Stability	±30 ppm
Aging	±20 ppm

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two−signal I^2C serial interface is provided. All the clock outputs can be individually enabled or disabled in a glitch free manner though this serial data interface. In addition, spread spectrum can be enabled for −0.35% or −0.5% down spread or no spread option can be selected though this interface. The registers associated with the serial interface initialize to their default settings upon power−up.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in Table 2 below.

Table 2. COMMAND CODE DEFINITION

Bit	Description

The block write and block read protocol is outlined in Table 3, while Table 4 outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 3. BLOCK READ AND BLOCK WRITE PROTOCOL

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
…	.....		
…	–		
…			
…			
		…	
…		…	
		…	

Table 4. BYTE READ AND BYTE WRITE PROTOCOL

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**

Table 13. ATTRIBUTES

Characteristic	Value
–	
	–

Table 14. ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Rating	Unit
		–	
		–	°

Table 16. AC ELECTRICAL CHARACTERISTICS ± – ° °

Table 17. AC ELECTRICAL CHARACTERISTICS − PCI EXPRESS JITTER SPECIFICATIONS

± − ° °

Symbol	Parameter	Test Condition	Spread Condition	Min	Typ	Max	PCIe Industry Spec	Unit
	− −	−	−					
		−	−					
		−	−					
			−					
		−						

− −
− −

−

PHASE NOISE

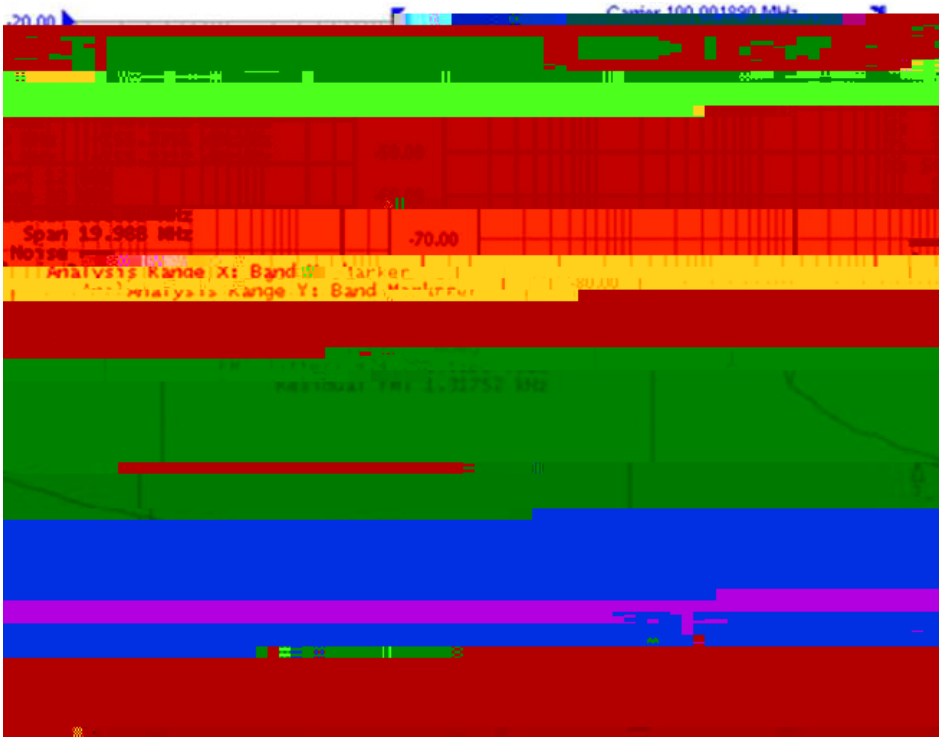


Figure 3. Typical Phase Noise Plot at 100 MHz (f_{CLKIN} = 25 MHz Crystal , f_{CLKOUT} = 100 MHz, RMS Phase Jitter = 424 fs for Integration Range of 12 kHz to 20 MHz, Output Termination = HCSL type)

APPLICATION INFORMATION

The outputs can be terminated to drive HCSL receiver (see Figure 6) or LVDS receiver (see Figure 7). HCSL output interface requires 49.9 termination resistors to GND for generating the output levels. LVDS output interface may not require the 100 near the LVDS receiver if the receiver has internal 100 termination. An optional series resistor R_L may be connected to reduce the overshoots in case of

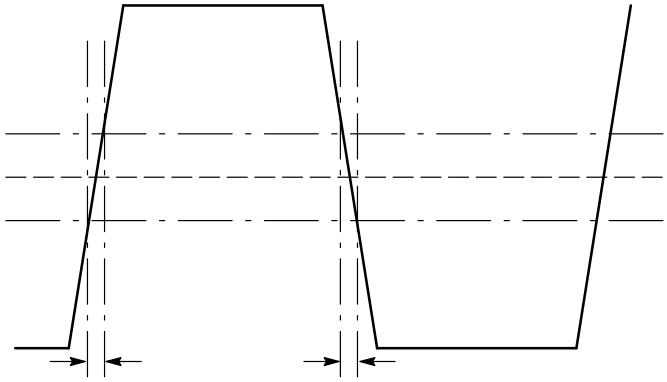


Figure 8. HCSL Differential Measurement of t_R/t_F

ORDERING INFORMATION

Device	Temperature	Package	Shipping
	– ° °	– –	

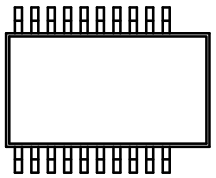
CASE 948H
ISSUE B

DATE 21 JUN 2012

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.08 MAX AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	---	1.20
1	0.0	0.1
	0.1	0. 0
	0.0	0.20
	. 0	0

1	. 0	. 0
	0.	
	0. 0	0.
2	0.2	
	0°	°



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