3.3 V 100/133 MHz Differential 1:19 HCSL Clock ZDB/Fanout Buffer for PCIe®

NB3N1900K

QFN72
MN SUFFIX
CASE 485DK

MARKING DIAGRAM*

Description

The NB3N1900K differential clock buffers are designed to work in conjunction with a PCIe compliant source clock synthesizer to provide point−to−point clocks to multiple agents. The device is capable of distributing the reference clocks for Intel® QuickPath Interconnect (Intel QPI & UPI), PCIe Gen1, Gen2, Gen3, Gen4. The NB3N1900K internal PLL is optimized to support 100 MHz and 133 MHz frequency operation. The NB3N1900K supports HCSL output levels.

Features

- Fixed Feedback Path for Lowest Input−to−Output Delay
- Eight Dedicated OE# Pins for Hardware Control of Outputs
- PLL Bypass Configurable for PLL or Fanout Operation
- Selectable PLL Bandwidth
- Spread Spectrum Compatible: Tracks Input Clock Spreading for Low EMI
- SMBus Programmable Configurations
- 100 MHz and 133 MHz PLL Mode to Meet the Next Generation PCIe Gen2/Gen3/Gen4 and Intel QPI & UPI Phase Jitter
- 2 Tri−Level Addresses Selection (Nine SMBUS Addresses)
- Cycle−to−Cycle Jitter: < 50 ps
- Output−to−Output Skew: < 65 ps
- Input−to−Output Delay: Fixed at 0 ps
- Input−to−Output Delay Variation: < 50 ps
- Phase Jitter: PCIe Gen3 < 1 ps rms
- Phase Jitter: PCIe Gen4 < 0.5 ps rms
- Phase Jitter: QPI 9.6GB/s < 0.12 ps rms
- QFN 72−pin Package, 10 mm x 10 mm
- These are Pb−Free Devices

ORDERING INFORMATION

See detailed ordering and shipping information on page 20 of this data sheet.

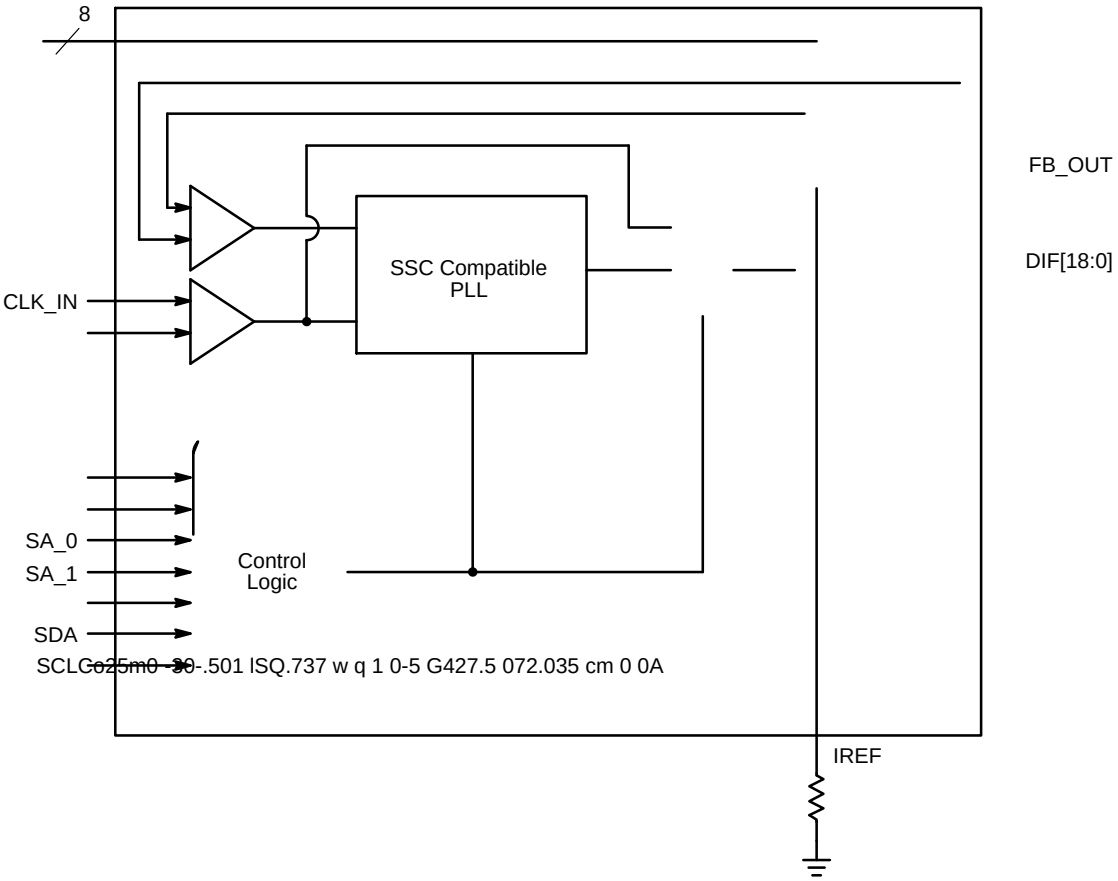

Figure 1. Simplified Block Diagram of NB3N1900K

NB3N1900K

Table 7. PIN DESCRIPTION

Pin #	Pin Name	Pin Type	Description
1	VDDA	PWR	3.3 V power for the PLL core.
2	GNDA	PWR	Ground pin for the PLL core.
3	IREF	OUT	This pin establishes the reference for the differential current−mode output pairs. It requires a fixed precision resistor to ground. 475 Ω is the standard value for 100 Ω differential impedance. Other impedances require different values. See data sheet.
4	100M_133M#	IN	Input to select operating frequency 1 = 100.00 MHz, 0 = 133.33 MHz
5	HBW_BYP_LBW#	IN	Trilevel input to select High BW, Bypass or Low BW mode. See PLL Operating Mode Table for Details.
6	PWRGD/PWRDN#	IN	Notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode.
7	GND	PWR	Ground pin.
8	VDDR	PWR	3.3 V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately.
9	CLK_IN	IN	0.7 V Differential true input
10	CLK_IN#	IN	0.7 V Differential complementary Input
11	SA_0	IN	SMBus address bit. This is a tri−level input that works in conjunction with the SA_1 to decode 1 of 9 SMBus Addresses.
12	SDA	I/O	Data pin of SMBus circuitry, 5V tolerant
13	SCL	IN	Clock pin of SMBus circuitry, 5V tolerant
14	SA_1	IN	SMBus address bit. This is a tri−level input that works in conjunction with the SA_0 to decode 1 of 9 SMBus Addresses.
15	NC	N/A	No Connection.
16	NC	N/A	No Connection.
17	FB_OUT#	OUT	Complementary half of differential feedback output, provides feedback signal to the PLL for synchronization with input clock to eliminate phase error.
18	FB_OUT	OUT	True half of differential feedback output, provides feedback signal to the PLL for synchronization with the input clock to eliminate phase error.
19	DIF0	OUT	0.7 V differential true clock output
20	DIF0#	OUT	0.7 V differential complementary clock output
21	VDD	PWR	Power supply, nominal 3.3 V
22	DIF1	OUT	0.7 V differential true clock output
23	DIF1#	OUT	0.7 V differential complementary clock output
24	DIF2	OUT	0.7 V differential true clock output
25	DIF2#	OUT	0.7 V differential complementary clock output
26	GND	PWR	Ground pin.
27	DIF3	OUT	0.7 V differential true clock output
28	DIF3#	OUT	0.7 V differential complementary clock output
29	DIF4	OUT	0.7 V differential true clock output
30	DIF4#	OUT	0.7 V differential complementary clock output
31	VDD	PWR	Power supply, nominal 3.3 V
32			

Table 7. PIN DESCRIPTION

Pin #	Pin Name	Pin Type	Description
38	DIF7	OUT	0.7 V differential true clock output
39	DIF7#	OUT	0.7 V differential complementary clock output
40	OE7#	IN	Active low input for enabling DIF pair 7. 1 = disable outputs, 0 = enable outputs
41	DIF8	OUT	0.7 V differential true clock output
42	DIF8#	OUT	0.7 V differential complementary clock output
43	OE8#	IN	Active low input for enabling DIF pair 8. 1 = disable outputs, 0 = enable outputs
44	GND	PWR	Ground pin.
45	VDD	PWR	Power supply, nominal 3.3 V
46	DIF9	OUT	0.7 V differential true clock output
47	DIF9#	OUT	0.7 V differential complementary clock output
48	OE9#	IN	Active low input for enabling DIF pair 9. 1 = disable outputs, 0 = enable outputs
49	DIF10	OUT	0.7 V differential true clock output
50	DIF10#	OUT	0.7 V differential complementary clock output
51	OE10#	IN	Active low input for enabling DIF pair 10. 1 = disable outputs, 0 = enable outputs
52	DIF11	OUT	0.7 V differential true clock output
53	DIF11#	OUT	0.7 V differential complementary clock output
54	OE11#	IN	Active low input for enabling DIF pair 11. 1 = disable outputs, 0 = enable outputs
55	DIF12	OUT	0.7 V differential true clock output
56	DIF12#	OUT	0.7 V differential complementary clock output
57	OE12#	IN	Active low input for enabling DIF pair 12. 1 = disable outputs, 0 = enable outputs
58	VDD	PWR	Power supply, nominal 3.3 V
59	DIF13	OUT	0.7 V differential true clock output
60	DIF13#	OUT	0.7 V differential complementary clock output
61	DIF14	OUT	0.7 V differential true clock output
62	DIF14#	OUT	0.7 V differential complementary clock output
63	GND	PWR	Ground pin.
64	DIF15	OUT	0.7 V differential true clock output
65	DIF15#	OUT	0.7 V differential complementary clock output
66	DIF16	OUT	0.7 V differential true clock output
67	DIF16#	OUT	0.7 V differential complementary clock output
68	VDD	PWR	Power supply, nominal 3.3 V
69	DIF17	OUT	0.7 V differential true clock output
70	DIF17#	OUT	0.7 V differential complementary clock output
71	DIF18	OUT	0.7 V differential true clock output
72	DIF18#	OUT	0.7 V differential complementary clock output

Table 8. ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	3.3 V Core Supply Voltage (Note 2)				4.6	V
V_{DD}	3.3 V Logic Supply Voltage (Note 2)				4.6	V
V_{IL}	Input Low Voltage		GND − 0.5			V
V_{IH}	Input High Voltage	Except for SMBus interface			V_{DD} + 0.5	V
V_{IHSMB}	Input High Voltage	SMBus clock and data pins			5.5	V
T_s	Storage Temperature		−65		150	°C
T_J	Junction Temperature				125	°C
T_c	Case Temperature				130	°C
ESD	ESD protection	Human Body Model	2000			V
θJA	Thermal Resistance Junction−to−Ambient	Still air		18.1		°C/W
θJC	Thermal Resistance Junction−to−Case			5.0		

Table 9. ELECTRICAL CHARACTERISTICS − INPUT/SUPPLY/COMMON PARAMETERS
(V_{DD} = V_{DDA} = 3.3 V ±5%, T_A = −10°C to +70°C), See Test Loads for Loading Conditions.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input High Voltage	Single−ended inputs, except SMBus, low threshold and tri−level inputs (Note 3)	2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	Single−ended inputs, except SMBus, low threshold and tri−level inputs (Note 3)	GND − 0.3		0.8	V
V_{IH_FS} (Note 4)	Input High Voltage		0.7		V_{DD} + 0.3	V
V_{IL_FS} (Note 4)	Input Low Voltage		GND − 0.3		0.35	V
I_{IN}	Input Current	Single−ended inputs, V_{IN} = GND, V_{IN} = V_{DD} (Note 3)	−5		5	μA
F_{IBYP}	Input Frequency	V_{DD} = 3.3 V, Bypass mode (Notes 3, 5 and 6)	33		400	MHz
F_{IPLL}		V_{DD} = 3.3 V, 100.00 MHz PLL mode (Note 5)	99	100.00	101	MHz
F_{IPLL}		V_{DD} = 3.3 V, 133.33 MHz PLL mode (Notes 5)	132.33	133.33	134.33	MHz
L_{PIN}	Pin Inductance	(Note 3)			7	nH
C_{IN}	Capacitance	Logic Inputs, except CLK_IN (Note 3)	1.5		5	pF
C_{INDIF_IN}		CLK_IN differential clock inputs (Notes 3 and 7)	1.5		2.7	pF
C_{OUT}		Output pin capacitance (Note 3)			6	pF
T_{STAB}	Clk Stabilization	From V_{DD} Power−Up and after input clock stabilization or de−assertion of PD# to 1st clock (Notes 3 and 5)			1.8	ms
f	Input SS Modulation Frequency	Allowable Frequency (Triangular Modulation) (Note 3)	30		33	kHz
$t_{LATOE\#}$	OE# Latency	DIF start after OE# assertion DIF stop after OE# de−assertion (Note 3)	4		12	cycles
t_{DRVPD}	Tdrive_PD#	DIF output enable after PD# de−assertion (Note 3)			300	μs
t_F	Tfall	Fall time of control inputs (Notes 3 and 5)			5	ns
t_R	Trise	Rise time of control inputs (Notes 3 and 5)			5	ns
V_{ILSMB}	SMBus Input Low Voltage	(Note 3)			0.8	V
V_{IHSMB}	SMBus Input High Voltage	(Note 3)	2.1		V_{DDSMB}	V
V_{OLSMB}	SMBus Output Low Voltage	@ I_{PULLUP} (Note 3)			0.4	V
I_{PULLUP}	SMBus Sink Current	@ V_{OL} (Note 3)	4			mA
V_{DDSMB}	Nominal Bus Voltage	3 V to 5 V ±10% (Note 3)	2.7		5.5	V
t_{RSMB}	SCL/SDA Rise Time	(Max V_{IL} − 0.15) to (Min V_{IH} + 0.15) (Note 3)			1000	ns
t_{FSMB}	SCL/SDA Fall Time	(Min VIH + 0.15) to (Max V_{IL} − 0.15) (Note 3)			300	ns
f_{MAXSMB}	SMBus Operating Frequency	Maximum SMBus operating frequency (Notes 3 and 8)			100	kHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
3. Guaranteed by design and characterization, not tested in production.
4. 100M_133M# Frequency Select (FS).
5. Control input must be monotonic from 20% to 80% of input swing.
6. Fmax measured until output violates output duty cycle specifications and output V_{High}, V_{Low} specification.
7. CLK_IN input
8. The differential input clock must be running for the SMBus to be active.

Table 10. ELECTRICAL CHARACTERISTICS − CLOCK INPUT PARAMETERS
(V_{DD} = V_{DDA} = 3.3 V ±5%, T_A = −10°C to +70°C), See Test Loads for Loading Conditions.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IHDIF}	Input High Voltage − CLK_IN (Note 9)	Differential inputs (single−ended measurement)	600		1150	mV

Table 12. ELECTRICAL CHARACTERISTICS − CURRENT CONSUMPTION

(V_{DD} = V_{DDA} = 3.3 V ±5%, T_A = −10°C to +70°C), See Test Loads for Loading Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD3.3OP}$	Operating Supply Current (Note 19)	All outputs active @ 100.00 MHz, C_L = Full load			550	mA
$I_{DD3.3PDZ}$	Powerdown Current (Note 19)	All differential pairs tri−stated			36	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

19. Guaranteed by design and characterization, not tested in production.

Table 13. ELECTRICAL CHARACTERISTICS − SKEW AND DIFFERENTIAL JITTER PARAMETERS

(V_{DD} = V_{DDA} = 3.3 V ±5%, T_A = −10°C to +70°C), See Test Loads for Loading Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SPO_PLL}	CLK_IN, DIF[x:0] (Notes 20, 21, 23, 24 and 27)	Input−to−Output Skew in PLL mode nominal value @ 25°C, 3.3 V	−100		100	ps
t_{PD_BYP}	CLK_IN, DIF[x:0] (Notes 20, 21, 22, 24 and 27)	Input−to−Output Skew in Bypass mode nominal value @ 25°C, 3.3 V	2.5		4.5	ns
t_{DSPO_PLL}	CLK_IN, DIF[x:0] (Notes 20, 21, 22, 24 and 27)	Input−to−Output Skew Variation in PLL mode across voltage and temperature			|100|	ps
t_{DSPO_BYP}	CLK_IN, DIF[x:0] (Notes 20, 21, 22, 24 and 27)	Input−to−Output Skew Variation in Bypass mode across voltage and temperature	−250		250	ps
t_{SKEW_ALL}	DIF{x:0] (Notes 20, 21, 22 and 27)	Output−to−Output Skew across all outputs (Common to Bypass and PLL mode)			65	ps
$j_{peak-hibw}$	PLL Jitter Peaking (Notes 26 and 27)	HBW_BYP_LBW# = 1	0		2.5	dB
$j_{peak-lobw}$	PLL Jitter Peaking (Notes 26 and 27)	HBW_BYP_LBW# = 0	0		2	dB
pll_{HIBW}	PLL Bandwidth (Notes 27 and 28)	HBW_BYP_LBW# = 1	2		4	MHz
pll_{LOBW}	PLL Bandwidth (Notes 27 and 28)	HBW_BYP_LBW# = 0	0.7		1.4	MHz
t_{DC}	Duty Cycle (Notes 20 and 27)	Measured differentially, PLL Mode	45	50	55	%
t_{DCD}	Duty Cycle Distortion (Notes 20 and 29)	Measured differentially, Bypass Mode @ 100.00 MHz	−2	0	2	%
$t_{jcyc-cyc}$	Jitter, Cycle to cycle (Notes 20, 27 and 30)	PLL mode			50	ps
		Additive Jitter in Bypass Mode			50	ps

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

20. Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.
21. Measured from differential cross−point to differential cross−point. This parameter can be tuned with external feedback path, if present.
22. All Bypass Mode Input−to−Output specs refer to the timing between an input edge and the specific output edge created by it.
23. This parameter is deterministic for a given device.
24. Measured with scope averaging on to find mean value. CLK_IN slew rate must be matched to DIF output slew rate.
25. t is the period of the input clock.
26. Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.
27. Guaranteed by design and characterization, not tested in production.
28. Measured at 3 db down or half power point.
29. Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode. @ 100.00 MHz.
30. Measured from differential waveform.

Table 14. ELECTRICAL CHARACTERISTICS − PHASE JITTER PARAMETERS
(V_{DD} = V_{DDA} = 3.3 V ±5%, T_A = −10°C to +70°C), See Test Loads for Loading Conditions.

Symbol	Parameter	Conditions (Notes 31 and 36)	Min	Typ	Max	Unit
$t_{jphPCIeG1}$	Jitter, Phase	PCIe Gen 1 (Notes 32 and 33)		12	86	ps (p−p)
$t_{jphPCIeG2}$		PCIe Gen 2 Lo Band 10 kHz < f < 1.5 MHz (Note 32)		0.2	3	ps (rms)
		PCIe Gen 2 High Band 1.5 MHz < f < Nyquist (50 MHz) (Note 32)		1.0	3.1	ps (rms)
$t_{jphPCIeG3}$		PCIe Gen 3 (PLL BW of 2−4 MHz, CDR = 10 MHz) (Note 32)		0.29	1	ps (rms)
$t_{jphPCIeG4}$		PCIe Gen 4 (PLL BW of 2−4 MHz, CDR = 10 MHz)		0.29	0.5	ps (rms)
t_{jphUPI}		UPI (9.6 Gb/s, 10.4 Gb/s or 11.2 Gb/s, 100 MHz, 12 UI)		0.7	1.0	ps (rms)
t_{jphQPI_SMI}		QPI & SMI (100.00 MHz or 133.33 MHz, 4.8 Gb/s, 6.4 Gb/s 12UI) (Note 34)		0.3	0.5	ps (rms)
		QPI & SMI (100.00 MHz, 8.0 Gb/s, 12UI) (Note 34)		0.1	0.3	ps (rms)
		QPI & SMI (100.00 MHz, 9.6 Gb/s, 12UI) (Note 34)		0.08	0.12	ps (rms)
$t_{jphPCIeG1}$	Additive Phase Jitter, Bypass mode	PCIe Gen 1 (Notes 32 and 33)			10	ps (p−p)
$t_{jphPCIeG2}$		PCIe Gen 2 Lo Band 10 kHz < f < 1.5 MHz (Notes 32 and 35)			0.3	ps (rms)
		PCIe Gen 2 High Band 1.5 MHz < f < Nyquist (50 MHz) (Notes 32 and 35)			0.7	ps (rms)
$t_{jphPCIeG3}$		PCIe Gen 3 (PLL BW of 2−4 MHz, CDR = 10 MHz) (Notes 32 and 35)			0.3	ps (rms)
t_{jphQPI_SMI}		QPI & SMI (100.00 MHz or 133.33 MHz, 4.8 Gb/s, 6.4 Gb/s 12UI) (Notes 34 and 35)			0.3	ps (rms)
		QPI & SMI (100.00 MHz, 8.0 Gb/s, 12UI) (Notes 34 and 35)			0.1	ps (rms)
		QPI & SMI (100.00 MHz, 9.6 Gb/s, 12UI) (Notes 34 and 35)			0.1	ps (rms)

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
31. Applies to all outputs.
32. See http://www.pcisig.com for complete specs
33. Sample size of at least 100K cycles. This figures extrapolates to 108 ps pk−pk @ 1M cycles for a BER of 1−12.
34. Calculated from Intel−supplied Clock Jitter Tool v 1.6.3.
35. For RMS figures, additive jitter is calculated by solving the following equation: (Additive jitter)^2 = (total jitter)^2 - (input jitter)^2
36. Guaranteed by design and characterization, not tested in production

Table 15. CLOCK PERIODS − DIFFERENTIAL OUTPUTS WITH SPREAD SPECTRUM DISABLED

		Measurement Window								
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
SSC OFF	Center Freq. MHz	−c2c jitter AbsPer Min	−SSC Short−Term Average Min	− ppm Long−Term Average Min	0 ppm Period Nominal	+ ppm Long− Term Average Max	+SSC Short−Term Average Max	+c2c jitter AbsPer Max	Unit	Notes
DIF	100.00	9.94900		9.99900	10.00000	10.00100		10.05100	ns	37, 38, 39
	133.33	7.44925		7.49925	7.50000	7.50075		7.55075	ns	37, 38, 40

37. Guaranteed by design and characterization, not tested in production.
38. All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ/CK410B+ accuracy requirements (±100 ppm). The 9ZX21901 itself does not contribute to ppm error.
39. Driven by SRC output of main clock, 100.00 MHz PLL Mode or Bypass mode
40. Driven by CPU output of main clock, 133.33 MHz PLL Mode or Bypass mode

Table 16. CLOCK PERIODS − DIFFERENTIAL OUTPUTS WITH SPREAD SPECTRUM ENABLED

		Measurement Window								
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
SSC ON	Center Freq. MHz	−c2c jitter AbsPer Min	−SSC Short−Term Average Min	− ppm Long−Term Average Min	0 ppm Period Nominal	+ ppm Long−Term Average Max	+SSC Short−Term Average Max	+c2c jitter AbsPer Max	Unit	Notes
DIF	99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns	41, 42, 43
	133.00	7.44930	7.49930	7.51805	7.51880	7.51955	7.53830	7.58830	ns	41, 42, 44

41. Guaranteed by design and characterization, not tested in production.
42. All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ/CK410B+ accuracy requirements (±100 ppm). The 9ZX21901 itself does not contribute to ppm error.
43. Driven by SRC output of main clock, 100.00 MHz PLL Mode or Bypass mode
44. Driven by CPU output of main clock, 133.33 MHz PLL Mode or Bypass mode

Table 17. POWER MANAGEMENT TABLE

Inputs		Control Bits/Pins				Outputs	
PWRGD/PWRDN#	CLK_IN/CLK_IN#	SMBus EN bit	OE# Pin	DIF(5:12) / DIF(5:12)#	Other DIF/ DIF#	FB_OUT / FB_OUT#	PLL State
0	X	X					

Figure 3. NB3N1900K Differential Test Loads

Table 18. DIFFERENTIAL OUTPUT TERMINATION TABLE

DIF Zo (Ω)	Iref (Ω)	Rs (Ω)	Rp (Ω)
100	475	33	50
85	412	27	42.2 or 43.2

PWRGD/PWRDN#

PWRGD/PWRDN# is a dual function pin. PWRGD is asserted high and de−asserted low. De−assertion of PWRGD (pulling the signal low) is equivalent to indicating a powerdown condition. PWRGD (assertion) is used by the NB3N1900K to sample initial configurations such as frequency select condition and SA selections.

After PWRGD has been asserted high for the first time, the pin becomes a PWRDN# (Power Down) pin that can be used to shut off all clocks cleanly and instruct the device to invoke power savings mode.

GENERAL SMBUS SERIAL INTERFACE INFORMATION FOR THE NB3N1900K

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $XX_{(H)}$
- Clock(device) will ***acknowledge***
- Controller (host) sends the beginning byte location = N
- Clock(device) will ***acknowledge***
- Controller (host) sends the data byte count = X
- Clock(device) will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X 1***
- Clock(device) will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

Table 21. INDEX BLOCK WRITE OPERATION

Controller (Host)		Clock (Device)	
T	starT bit		
Slave Address $XX_{(H)}$			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
Data Byte Count = X			
		ACK	
Beginning Byte N			
		X Byte	ACK
O			O
O			O
			O
Byte N + X - 1			
		ACK	
P	stoP bit		

Note: $XX_{(H)}$ is defined by SMBus address select pins

How to ReadTm-001 Tc-0001 Tw[GENERAL)17/F1 1 09 15.364 hmy5pAge1294.071 1

Table 23. SMBusTable: PLL MODE, AND FREQUENCY SELECT REGISTER

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	5	PLL Mode 1	PLL Operating Mode Rd back 1	R	See PLL Operating Mode Readback Table		Latch
Bit 6	5	PLL Mode 0	PLL Operating Mode Rd back 0	R			Latch
Bit 5	72/71	DIF_18_En	Output Control overrides OE# pin	RW	Hi−Z	Enable	1
Bit 4	70/69	DIF_17_En	Output Control overrides OE# pin	RW	Hi−Z	Enable	1
Bit 3	67/66	DIF_16_En	Output Control overrides OE# pin	RW	Hi−Z	Enable	1
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0	4	100M_133M#	Frequency Select Readback	R	133 MHz	100 MHz	Latch

Table 24. SMBusTable: OUTPUT CONTROL REGISTER

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	39/38	DIF_7_En	Output Control overrides OE# pin	RW	Hi−Z	Enable	1
Bit 6	35/36	DIF_6_En	Output Control overrides OE# pin	RW			1
Bit 5	32/33	DIF_5_En	Output Control overrides OE# pin	RW			1
Bit 4	29/30	DIF_4_En	Output Control overrides OE# pin	RW			1
Bit 3	27/28	DIF_3_En	Output Control overrides OE# pin	RW			1
Bit 2	24/25	DIF_2_En	Output Control overrides OE# pin	RW			1
Bit 1	22/23	DIF_1_En	Output Control overrides OE# pin	RW			1
Bit 0	19/20	DIF_0_En	Output Control overrides OE# pin	RW			1

Table 25. SMBusTable: OUTPUT CONTROL REGISTER

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	65/64	DIF_15_En	Output Control overrides OE# pin	RW	Hi−Z	Enable	1
Bit 6	62/61	DIF_14_En	Output Control overrides OE# pin	RW			1
Bit 5	60/59	DIF_13_En	Output Control overrides OE# pin	RW			1
Bit 4	56/55	DIF_12_En	Output Control overrides OE# pin	RW			1
Bit 3	53/52	DIF_11_En	Output Control overrides OE# pin	RW			1

Table 27. SMBusTable: RESERVED REGISTER

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

Table 28. SMBusTable: VENDOR & REVISION ID REGISTER

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	−	RID3	REVISION ID	R	–		X
Bit 6	−	RID2		R			X
	−						

Table 31. SMBusTable: RESERVED REGISTER

Byte 8	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0

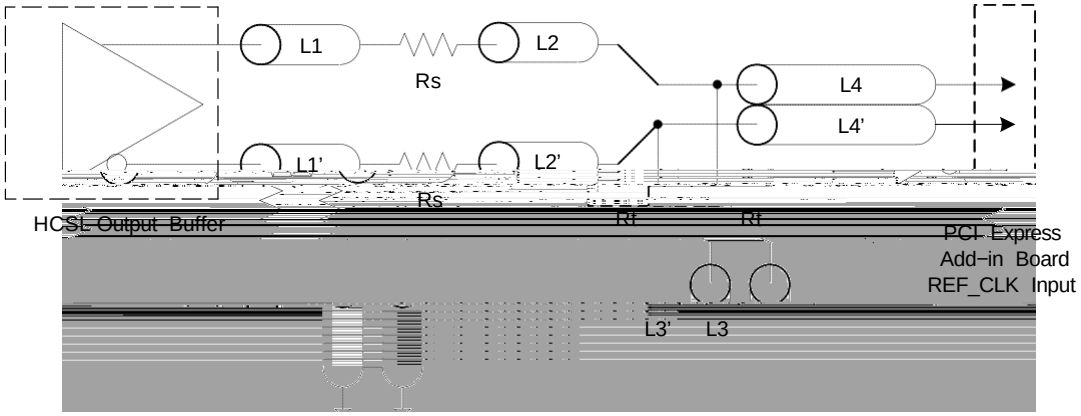

Figure 7. PCI Express Connector Routing

Table 32. ALTERNATIVE TERMINATION FOR LVDS AND OTHER COMMON DIFFERENTIAL SIGNALS (Figure 8)

Vdiff (V)	Vpp (V)	Vcm (V)	R1 (Ω)	R2 (Ω)	R3 (Ω)	R4 (Ω)	Note
0.45	0.22	1.08	33	150	100	100	
0.58	0.28	0.6	33	78.7	137	100	
0.60	0.3	1.2	33	174	140	100	Standard LVDS

R1a = R1b = R1
R2a = R2b = R2