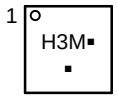
2.5 V Programmable OmniClock Generator

NB3H60113GH3

The NB3H60113GH3, which is a member of the OmniClock family, is a one−time programmable (OTP), low power PLL−based clock generator that supports differential 125 MHz frequency output. The device accepts a single ended LVCMOS reference Clock as input. It generates one differential LVDS output. The device can be powered down using the Power Down pin (PD#).



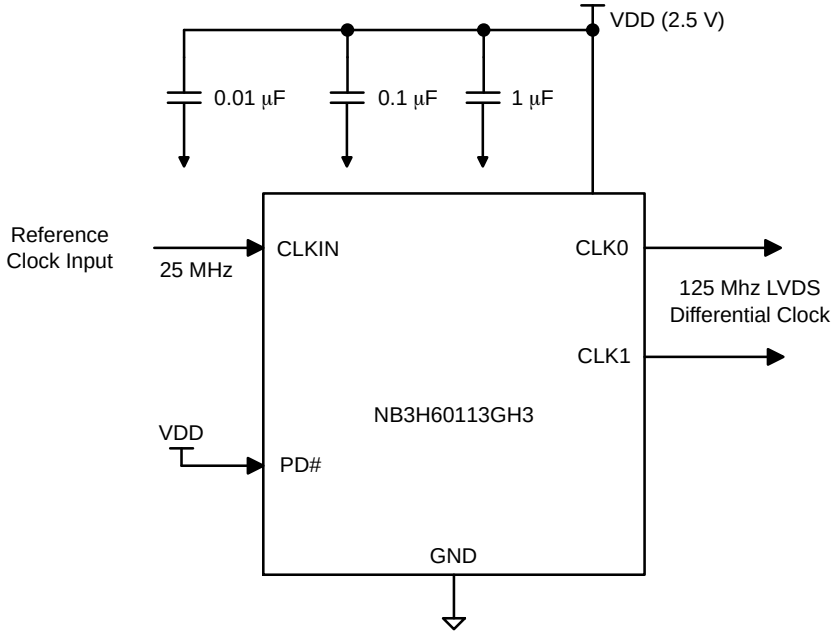
H3 = Specific Device Code
M = Date Code
▪ = Pb−Free Device

(Note: Microdot may be in either location)

See detailed ordering and shipping information on page 11 of this data sheet.

- Member of the OmniClock Family of Programmable Clock Generators
- Operating Power Supply: 2.5 V ± 10%
- I/O Standards
  - Input: LVCMOS Clock
  - Output: LVDS
- 1 Programmable Differential Clock Output of 125 MHz
- Input Frequency Range
  - Reference Clock: 25 MHz
- Power Saving mode through Power Down Pin
- Programming and Evaluation Kit for Field Programming and Quick Evaluation
- Temperature Range −40°C to 85°C
- Packaged in 8−Pin WDFN
- These are Pb−Free Devices

- Telecom Networks



Power Down

Power saving mode can be activated through the power down PD# input pin. This input is an LVCMOS active Low Master Reset that disables the device and sets outputs Low. By default it has an internal pull−down resistor. The chip functions are disabled by default and when PD# pin is pulled high the chip functions are activated.

NB3H60113GH3 has one Configuration. Table 3 shows the device configuration.

25 MHz	CLK0 = 125 MHz CLK1 = 125 MHz	2.5 V	CLK0 = Y CLK1 = Y	CLK0/CLK1 = LVDS CLK2: NC

ESD Protection Human Body Model	2 kV
Internal Input Default State Pull up/ down Resistor	50 kΩ
Moisture Sensitivity, Indefinite Time Out of Dry Pack (Note 1)	MSL1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count	130 k
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

(Note 2)

VDD	Positive power supply with respect to Ground	−0.5 to +4.6	V
V_I, V_O	Input / Output Voltage with respect to chip ground	−0.5 to VDD + 0.5	V
T_A	Operating Ambient Temperature Range (Industrial Grade)	−40 to +85	°C
T_{STG}	Storage temperature	−65 to +150	°C
T_{SOL}	Max. Soldering Temperature (10 sec)	265	°C
θ_{JA}	Thermal Resistance (Junction−to−ambient) 0 lfpm (Note 3) 500 lfpm	129 84	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−case)	35 to 40	°C/W
T_J	Junction temperature	125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

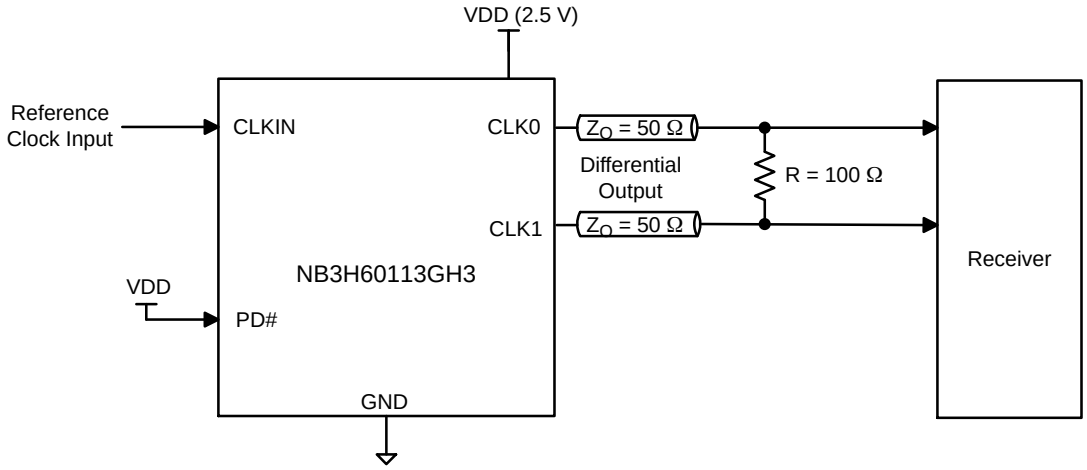
2. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power). ESD51.7 type board. Back side Copper heat spreader area 100 sq mm, 2 oz (0.070 mm) copper thickness.

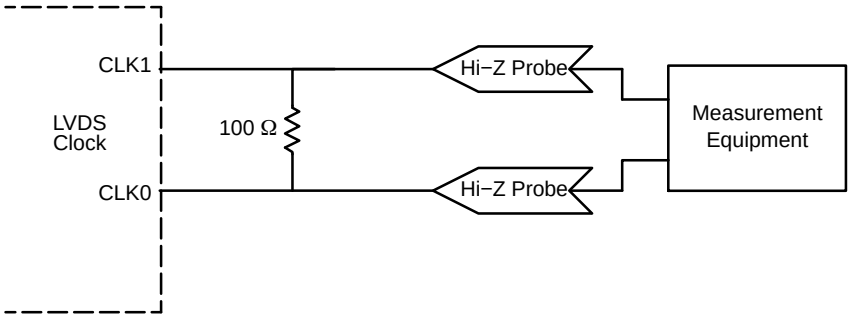
V_{DD}	Core Power Supply Voltage	2.5 V operation	2.25	2.5	2.75	V
fclkin	Reference Clock Frequency	Single ended clock Input		25		MHz

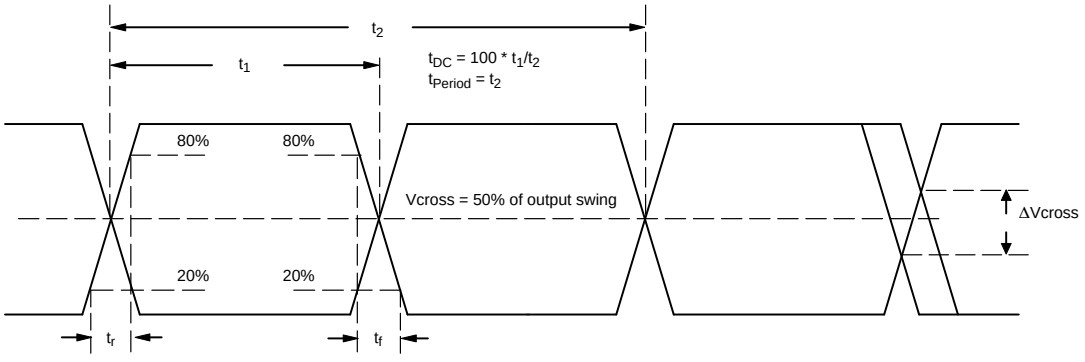
Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

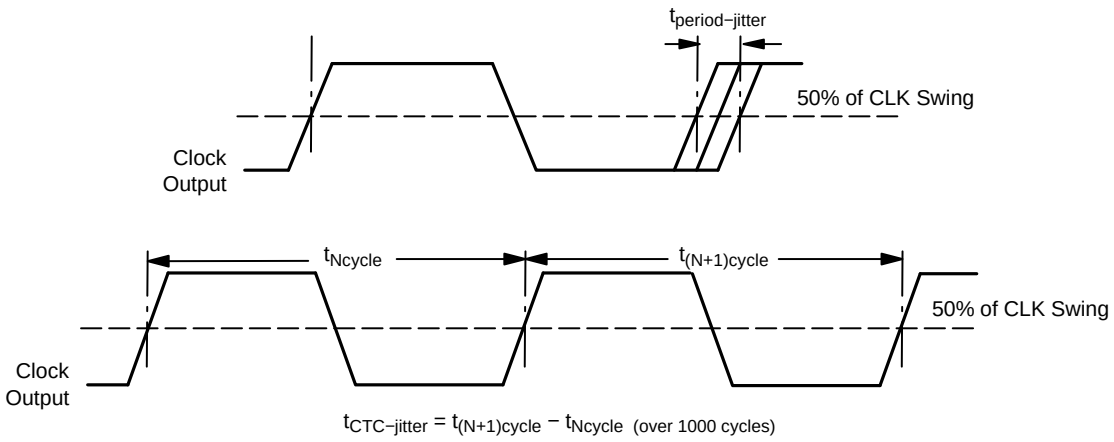
(V_{DD} = 2.5 V ± 10%; GND = 0 V, T_A = −

(V_{DD} = 2.5 V ± 10%, GND = 0 V, T_A = −40°C to 85°C, Note 10)


VDD (2.5 V)
Reference
Clock Input
CLKIN
CLK0
Z_O = 50 Ω
Differential
Output
R = 100 Ω
CLK1
Z_O = 50 Ω
Receiver
NB3H60113GH3
VDD
PD#
GND


CLK1
Hi−Z Probe
LVDS
Clock
100 Ω
Measurement
Equipment
CLK0
Hi−Z Probe


t_2
t_1
$t_{DC} = 100 * t_1/t_2$
$t_{Period} = t_2$
80%
80%
Vcross = 50% of output swing
ΔVcross
20%
20%
t_r
t_f



$t_{CTC-jitter} = t_{(N+1)cycle} - t_{Ncycle}$ (over 1000 cycles)

and measurement techniques of Cycle−cycle jitter, period jitter, TIE jitter and Phase Noise are explained in application note AND8459/D.

In order to have a good clock signal integrity for minimum data errors, it is necessary to reduce the signal reflections. Reflection coefficient can be zero only when the source impedance equals the load impedance. Reflections are based on signal transition time (slew rate) and due to impedance mismatch. Impedance matching with proper termination is required to reduce the signal reflections. The amplitude of overshoots is due to the difference in impedance and can be minimized by adding a series resistor (Rs) near the output pin. Greater the difference in impedance, greater is the amplitude of the overshoots and subsequent ripples. The ripple frequency is dependant on the signal travel time from the receiver to the source. Shorter traces results in higher ripple frequency, as the trace gets longer the travel time