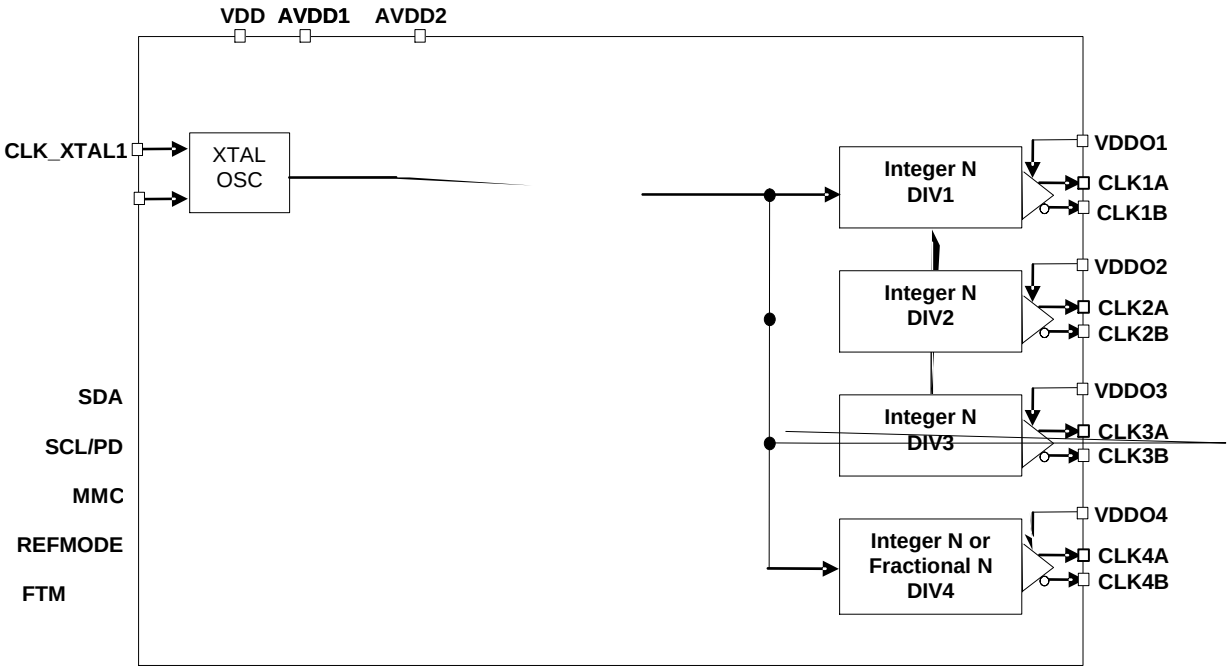

VDD
AVDD1
AVDD2
CLK_XTAL1
XTAL OSC
SDA
SCL/PD
MMC
REFMODE
FTM
Integer N DIV1
Integer N DIV2
Integer N DIV3
Integer N or Fractional N DIV4
VDDO1
CLK1A
CLK1B
VDDO2
CLK2A
CLK2B
VDDO3
CLK3A
CLK3B
VDDO4
CLK4A
CLK4B

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	$\overline{\text{CLK}}$_XTAL2	Crystal or LVPECL/LVDS Input	Crystal Output or Differential Clock Input (complementary); If CLK_XTAL1 is used as single−ended input, $\overline{\text{CLK}}$_XTAL2 must be connected to ground. See Table 2.
2	REFMODE	LVTTL/LVCMOS Input	Reference Input Select to either use a crystal, or overdrive with a single−ended or differential input; see Table 2. Internal pull−down.
3	SDA	LVTTL/LVCMOS Input	Serial Data Input for I2C/SMBus compatible; Defaults High when left open; internal pull−up. 5V tolerant.
4	SCL/PD	LVTTL/LVCMOS Input	Serial Clock Input for I2C/SMBus compatible; Defaults High when left open; internal pull−up. SCL/PD is also a device power−down pin (when High) in pin−strap mode only. 5V tolerant.
5	VDD	Power	3.3 V / 2.5 V Positive Supply Voltage for the Inputs and Core
6	FS1	LVTTL/LVCMOS Input	Frequency Select 1 for DIV1, CLK1A & CLK1B; Three–level input buffer; Default is mid−logic level; internal RPull−up and RPull−down. See Table 3.
7	FS2	LVTTL/LVCMOS Input	Frequency Select 2 for DIV2, CLK2A & CLK2B; Three–level input buffer; Default is mid−logic level; internal RPull−up and RPull−down. See Table 3.
8	FS3	LVTTL/LVCMOS Input	Frequency Select 3 for DIV3, CLK3A, & CLK3B; Three–level input buffer; Default is mid−logic level; internal RPull−up and RPull−down. See Table 3.
9	FS4A	LVTTL/LVCMOS Input	Frequency Select 4A for DIV4, CLK4A & CLK4B; Three–level input buffer; Default is mid−logic level; internal RPull−up and RPull−down. See Table 4.
10	FS4B	LVTTL/LVCMOS Input	Frequency Select 4B for DIV4, CLK4A & CLK4B; Three–level input buffer; Default is mid−logic level; internal RPull−up and RPull−down. See Table 4.
11	LDO4	Power	1.8 V LDO − Install Power Conditioning Bypass Capacitor to Ground
12	AVDD3	Power	3.3 V / 2.5 V Positive Supply Voltage for Analog circuits. AVDD3 = VDD.
13	LDO3	Power	1.8V LDO − Install Power Conditioning Bypass Capacitor to Ground
14	CLK4A	Output	LVCMOS (single−ended) or Non− Inverted Differential LVPECL Clock A for Channel 4 Output
15	CLK4B	Output	LVCMOS (single−ended) or Inverted Differential LVPECL Clock B for Channel 4 Output
16	VDDO4	Power	3.3 V / 2.5 V / 1.8 V Positive Supply Voltage for the CLK4A/4B Outputs
17	MMC	LVTTL/LVCMOS Input	Mix Mode Control Pin for use as a combination of FSn settings and I2C setting for the CLK(n) outputs in the I2C mode; see Table 5. No logic level default; use a RPull−up resistor for High or a RPull−down resistor for Low.
18	CLK3B	Output	LVCMOS (single−ended) or Inverted Differential LVPECL Clock B for Channel 3 Output
19	CLK3A	Output	LVCMOS (single−ended) or Non−Inverted Differential LVPECL Clock A for Channel 3 Output
20	VDDO3	Power	3.3 V / 2.5 V / 1.8 V Positive Supply Voltage for the CLK3A/3B Outputs
21	VDDO2	Power	3.3 V / 2.5 V / 1.8 V Positive Supply Voltage for the CLK2A/2B Outputs
22	CLK2A	Output	LVCMOS (single−ended) or Non− Inverted Differential LVPECL Clock A for Channel 2 Output
23	CLK2B	Output	LVCMOS (single−ended) or Inverted Differential LVPECL Clock B for Channel 2 Output
24	FTM		Factory Test Mode. Must connect this pin to Ground.
25	VDDO1	Power	3.3 V / 2.5 V / 1.8 V Positive Supply Voltage for the CLK1A/1B Outputs
26	CLK1B	Output	LVCMOS (single−ended) or Inverted Differential LVPECL Clock B for Channel 1 Output
27	CLK1A	Output	LVCMOS (single−ended) or Non−Inverted Differential LVPECL Clock A for Channel 1 Output
28	AVDD2	Power	3.3 V / 2.5 V Positive Supply Voltage for Analog circuits. AVDD2 = VDD.
29	LDO2	Power	1.8 V LDO − Install Power Conditioning Bypass Capacitor to Ground
30	AVDD1	Power	3.3 V / 2.5 V Positive Supply Voltage for Analog circuits. AVDD1 = VDD.
31	LDO1	Power	1.8 V LDO − Install Power Conditioning Bypass Capacitor to Ground

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
32	CLK_XTAL1	Crystal or LVTTL/LVCMOS or LVPECL/LVDS Input	Crystal Input or Single−Ended or Differential Clock Input; If CLK_XTAL1 is used as single−ended input, $\overline{\text{CLK}}$_XTAL2 must be connected to ground. See Table 2.
EP	Exposed Pad	Ground	Ground – Negative Power Supply is connected via the Exposed Pad . The Exposed Pad (EP) on the QFN−32 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat sinking conduit. The pad is electrically connected to the die,carries all power supply return currents and must be electrically connected to GND.

1. All VDD, AVDDn, VDDOn, EP (GND) pins must be externally connected to a power supply for proper operation. VDD and AVDDn must all be at the same voltage.

NB3H5150 BASIC OPERATION

Introduction

The NB3H5150 is a Multi−Rate Clock Generator. The clock reference for the PLL can be either a 25 MHz crystal, single−ended LVCMOS or LVTTL signal or a differential LVPECL, LVDS or HCSL signal.

There are two modes of operation for the NB3H5150, Pin−Strap and I^2C.

In the **Pin−Strap Mode**, the user can select any of the defined output frequencies for each of the four output banks as specified in Tables 3 and 4 via the three−level Frequency Select pins: FS1, FS2, FS3, FS4A and FS4B.

In the **I^2C mode**, the user can select one of the approved register files. Each register file is an expanded selection of output frequencies and level combinations, output enable/disable and bypass mode functions.

CLKnA & CLKnB − Output Frequency and Output Level Selection

There are four output banks: CLK1A&B, CLK2A&B and CLK3A&B are integer only divider outputs, whereas CLK4A&B can be set or programmed as an integer or fractional divider.

The output levels for each output bank can be LVPECL (differential) or LVCMOS (two single−ended). Output Enable / Disable functions are available in I^2C only.

CLK1, 2, 3 and 4 outputs are not phase−aligned, in PLL or PLL bypass modes.

Power−On Output Default

Upon power−up, all four outputs will be forced to and held at static LVPECL levels (CLKnA = Low, CLKnB = High) until the PLL is stable. The PLL will be stable before any of the output Clocks, CLKnx, are enabled.

SDA & SCL/PD − Serial Data Interface – I2C

The NB3H5150 incorporates a two−wire Serial Data Interface to expand the flexibility and function of the NB3H5150 clock generator.

The I^2C interface pins, SCL and SDA, are used to load register files into the NB3H5150.

These register files will configure the internal registers to achieve an expanded selection of output frequencies and levels combinations for each of the four output blocks.

Subsequent changes in the registers can then be performed with another register file to modify any of the output frequencies or output modes.

OE, Output Enable

An OE, Output Enable/Disable function is available only in the I^2C mode by loading a register file, such that any individual output bank can be enabled or disabled. In LVCMOS modes outputs will disable LOW for CLKnA and CLKnB, while the LVPECL mode outputs will disable CLKnA = Low and CLKnB = High.

Mixed Mode Control (MMC)

In the I^2C mode, the Mixed Mode Control (MMC) pin is used for a combination of FSn settings and I2C settings to control the CLK(n) outputs' function as defined in Table 5.

REFMODE – Select a Crystal or External Clock Input Interface (See Table 2)

The REFMODE pin will select the reference input for the CLK_XTAL1 and $\overline{\text{CLK}}$_XTAL2 pins to use either a crystal, an overdriven single−ended or differential input.

When using a crystal, set the REFMODE pin to a LOW. The CLK_XTAL1 and $\overline{\text{CLK}}$_XTAL2 input pins will accept a 25 MHz crystal.

When using a direct−coupled differential input, set the REFMODE pin to a HIGH.

When REFMODE is HIGH, the CLK_XTAL1 and $\overline{\text{CLK}}$_XTAL2 differential input pins have internal AC coupling capacitors selected with self−bias circuity for the differential input buffer. This differential buffer

become effective and will begin to output the selected frequencies.

2. Subsequent changes to any FS pin(s) will cause the associated CLK(n) output(s) to momentarily go to static levels, and then to resume at the new frequency; CLK(n) will follow the FS(n) pin programmable Tables 3 and 4 for output frequencies and interface levels.
   Note that in changing from LVPECL to LVCMOS (or vice−versa), output logic levels cannot be guaranteed. This is because the receiver inputs are not likely to change in a given application, and the LVPECL output loading in the application will also not change. It is logical to presume that the output type will be predetermined and fixed. Therefore, in a system/application, the user should be aware that subsequent change to the FS pin should only change frequency, and not output type.
3. Power off/on cycle will repeat the entire sequence
4. **Power Down**
   To initiate the Power−Down mode, the SDA pin must be LOW and remain LOW. If the SCL/PD pin is taken HIGH at any time, the device enters a complete power−down mode with a current consumption of less than 1 mA for the entire device. When SCL/PD is subsequently taken LOW, the device will function as though power were removed and re−applied. That is, sequencing will begin at #1.
   Power−down is also available via I^2C with a register file.

FS(n) Pin Programmable Selection of Output Frequencies and Levels

Table 3. NB3H5150 − CLK1A:3A & CLK1B:3B OUTPUT FREQUENCY SELECT TABLE WITH 25 MHz CRYSTAL

Logic Level	FS1 (CLK1) (MHz)	FS2 (CLK2) (MHz)	FS3 (CLK3) (MHz)
Low	50.00 (LVCMOS)	156.25 (LVPECL)	156.25 (LVPECL)
Mid / Float*	33.33 (LVCMOS)	25.00 (LVPECL)	125.00 (LVCMOS)
High	25.00 (LVCMOS)	125.00 (LVPECL)	100.00 (LVPECL)

*(Default)

Table 4. NB3H5150 − CLK4A & CLK4B OUTPUT FREQUENCY SELECT TRUTH

I²C MODE: (see Table 5)

Some features that are not available in pin−strap mode can be obtained in I2C mode, such as Output Enable/Disable, By−Pass

Table 5. SDA, SCL AND MMC CONTROL PINS FOR OUTPUT FUNCTION

Mode	SDA	SCL/PD	MMC	Comments	Outputs (Note 2)	
					CLK1, CLK2, CLK3	CLK4
Mixed Mode	H Note 4	H Note 4	L		Static LVPECL Logic Levels	Static LVPECL Logic Levels
	H Note 4	H Note 4	H FS4A = L		Static LVPECL Logic Levels	Active per Table 4
	H Note 4	H Note 4	H FS4A = M or H		Active per Table 3	Static LVPECL Logic Levels

2. All outputs are static until after the PLL is stable.
3. Any changes to the device configuration after power−up are made by reading and writing to registers through the I2C interface.
4. Don’t care state unless device address is matched by controller address.

X = don’t care

Table 6. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model Charge Device Model	> 2 kV > 150 V > 500 V
Moisture Sensitivity (Note 5) 32−QFN		Level 1
Flammability Rating Oxygen Index: 28 to 34		UL 94 V−0 @ 0.125 in
Transistor Count		245, 894
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

5. For additional information, see Application Note AND8003/D.

Table 7. MAXIMUM RATINGS

Symbol	Parameter		Condition	Rating	Unit
V_{DD}	Positive Power Supply – Core		GND = 0 V	3.63	V
AV_{DDn}	Positive Power Supply – Analog		GND = 0 V	3.63	V
V_{DDOn}	Positive Power Supply – Outputs		GND = 0 V	3.63	V
V_{IO}	Positive Input/Output Voltage		GND = 0 V	−0.5 to V_{DD} +0.5	V
V_I	Positive Input Voltage SDA and SCL		GND = 0 V	5.5	V
T_A	Operating Temperature Range		QFN−32	−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_J	Maximum Junction Temperature			125	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 6)	QFN−32 QFN−32	0 lfpm 500 lfpm	31 27	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case) (Note 6)	QFN−32		12	°C/W
T_J	Maximum Junction Temperature			125	°C
T_{sol}	Wave Solder Pb−Free, 10 sec			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
6. JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

Table 8. DC CHARACTERISTICS

V_{DD} = AV_{DDn} = 3.3 V ±5% or 2.5 V ±5%; V_{DDOn} = 3.3 V ±5% or 2.5 V ±5% or 1.8 V ±5%; GND = 0 V; T_A = −40°C to 85°C

Symbol	Characteristic		Min	Typ	Max	Unit
POWER SUPPLY / CURRENT (Note 12)						
V_{DD}/AV_{DDn}	Core Power Supply	V_{DD} = AV_{DDn} = 3.3 V	3.135	3.3	3.465	V
		V_{DD} = AV_{DDn} = 2.5 V	2.375	2.5	2.625	
V_{DDOn}	Output Power Supply	V_{DDOn} = 3.3 V	3.135	3.3	3.465	
		V_{DDOn} = 2.5 V	2.375	2.5	2.625	
		V_{DDOn} = 1.8 V (LVCMOS only)	1.71	1.8	1.89	
I_{DD}/I_{ADDn}	Core and Input Power Supply Current for V_{DD} and A_{VDDn}					
	V_{DD} = 3.3 V	CLK4 Integer				
		CLK4 Frac−N				
	V_{DD} = 2.5 V	CLK4 Integer				
		CLK4 Frac−N				

Table 8. DC CHARACTERISTICS

V_{DD} = AV_{DDn} = 3.3 V ±5% or 2.5 V ±5%; V_{DDOn} = 3.3 V ±5% or 2.5 V ±5% or 1.8 V ±5%; GND = 0 V; T_A = −40°C to 85°C

Symbol	Characteristic	Min	Typ	Max	Unit
LVCMOS OUTPUT; See Figure 12					
V_{OH}	Output HIGH Voltage IOH = 12 mA	V_{DDO} – 0.5		V_{DDO}	V
V_{OL}	Output LOW Voltage IOL = 12 mA	GND		0.5	V
R_{OUT}	Output Impedance		15		Ω
CRYSTAL INPUT DRIVEN SINGLE−ENDED (REFMODE = 1) (see Figure 3 and 5) (Note 9)					
V_{IHSE}	CLK_XTAL1 Single−Ended Input HIGH Voltage	200		V_{DD}	mV
V_{ILSE}	CLK_XTAL1 Single−Ended Input LOW Voltage	GND		V_{IHSE} − 200	mV
V_{th}	Input Threshold Reference Voltage Range	100		V_{DD} − 100	mV
V_{ISE}	Single−Ended Input Voltage (V_{IH} – V_{IL})	200		V_{DD}	mV
CRYSTAL INPUTS DRIVEN DIFFERENTIALLY (REFMODE = 1) (see Figure 4 and 6) (Note 11)					
V_{IHD}	Differential Input HIGH Voltage	100		V_{DD}	mV
V_{ILD}	Differential Input LOW Voltage	GND		V_{IHD} – 100	mV
V_{ID}	Differential Input Voltage (V_{IHD} – V_{ILD})	100		V_{DD}	mV
V_{CMR}	Input Common Mode Range (Differential Configuration) (Note 10) (Figure 8)	50		V_{DD} − 50	mV
I_{IH}	Input HIGH Current CLK_XTAL1 and CLKb_XTAL2	−10		10	μA
I_{IL}	Input LOW Current CLK_XTAL1 & CLKb_XTAL2	−10		10	μA
LVCMOS − CONTROL AND SDA & SCL/PD INPUTS					
V_{IH}	Input HIGH Voltage for MMC & REFMODE Pins	V_{DD}			

Table 9. AC CHARACTERISTICS

V_{DD} = AV_{DDn} = 3.3 V ±5% or 2.5 V ±5%; V_{DDO} = 3.3V ±5% or 2.5 V ±5% or 1.8 V ±5%; GND = 0 V; T_A = −40°C to 85°C (Note 13)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{CLKIN}	External Clock / Crystal Input Frequency − PLL Mode	−1000 ppm	25	+1000 ppm	MHz
f_{INBP}	External Clock Input Frequency – PLL Bypass Mode I^2C Mode; $f_{in} = f_{out}$	1		50	MHz
$f_{CLK1,2,3}$	CLK1, CLK2, CLK3 Typical Output Clock Frequencies; f_{in} = 25 MHz		25 33.33 50 100 125 156.25		MHz
f_{CLK4}	CLK4 Outputs Typical Output Clock Frequencies; f_{in} = 25 MHz Resolution of 1 Hz Integer Frac−N		66.66 106.23 133.33 155.52 161.1328		MHz
fSDA/SCL	Serial Data and Clock Rates		100k		bps
t_{PWSCL}	Serial Clock Pulse Width	1			μs
$t_{w\mu}$	Time SCL/PD Pin must be Held Low to “Wake−up” the Device	100			ns
t_{DC}	Output Clock Duty Cycle (Crystal or Reference Duty Cycle = 50%) PLL Mode; <1 ns t_r / t_f LVPECL f_{out} = 156.25 MHz LVCMOS f_{out} = 33.33 MHz PLL Bypass Mode; Input Duty Cycle = 50%, $V_{INPP} \geq$ 1.2 V	 47.5 47.5 45	 50 50	 52.5 52.5 55	%
Φ_N	Phase Noise (Integer−N) fout = 156.25 MHz, fin = 25 MHz Crystal, LVPECL 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz 20 MHz		 −115 −130 −140 −145 −153 −153		dBc
Φ_N	Phase Noise (Integer−N) fout = 100 MHz, fin = 25 MHz Crystal, LVCMOS 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz 20 MHz		 −120 −136 −142 −145 −156 −156		dBc
Φ_N	Phase Noise (Frac−N) fout = 155.52 MHz, fin = 25 MHz Crystal, LVPECL 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz 20 MHz		 −115 −127 −131 −135 −152 −153		dBc
Φ_N	Phase Noise (Frac−N) fout = 133.33 MHz, fin = 25 MHz Crystal, LVCMOS 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz 20 MHz		 −117 −126 −126 −131 −153 −153		dBc
$t_{jit}(\Phi)$	RMS Phase Jitter − 25 MHz Crystal (Note 15) Integration Range:12 kHz − 20 MHz fout = 156.25 MHz, Integer CLK_n fout = 155.52 MHz; Frac−N CLK4			 300 1000	fs
$t_{jit}(\Phi)$	Additive RMS Phase Jitter (PLL Bypass in I^2C Mode) Integration Range:12 kHz − 5 MHz fout = 25 MHz, CLK1 LVCMOS		50		fs
tpd	Input to Output Propagation Delay (PLL Bypass in I^2C Mode) 25 MHz		5		ns

Table 9. AC CHARACTERISTICS

V_{DD} = AV_{DDn} = 3.3 V ±5% or 2.5 V ±5%; V_{DDO} = 3.3V ±5% or 2.5 V ±5% or 1.8 V ±5%; GND = 0 V; T_A = −40°C to 85°C (Note 13)

Symbol	Characteristic	Min	Typ	Max	Unit
PSRR	Ripple Induced Phase Spur Level 100 kHz & 1 MHz, 100 mVpp, Ripple Injected on V_{DD}/AV_{DDn} ≤ 100 MHz		−60		dBc
t_r /t_f	Output Rise/Fall Times (CLKnA/CLKnB), 20% − 80% of $VDDO_n$ fout = 156.25 Mhz LVPECL fout = 33.33 Mhz @ VDDO = 3.3 V LVCMOS – 5 pF	 120 500	 200 800	 300 1000	ps

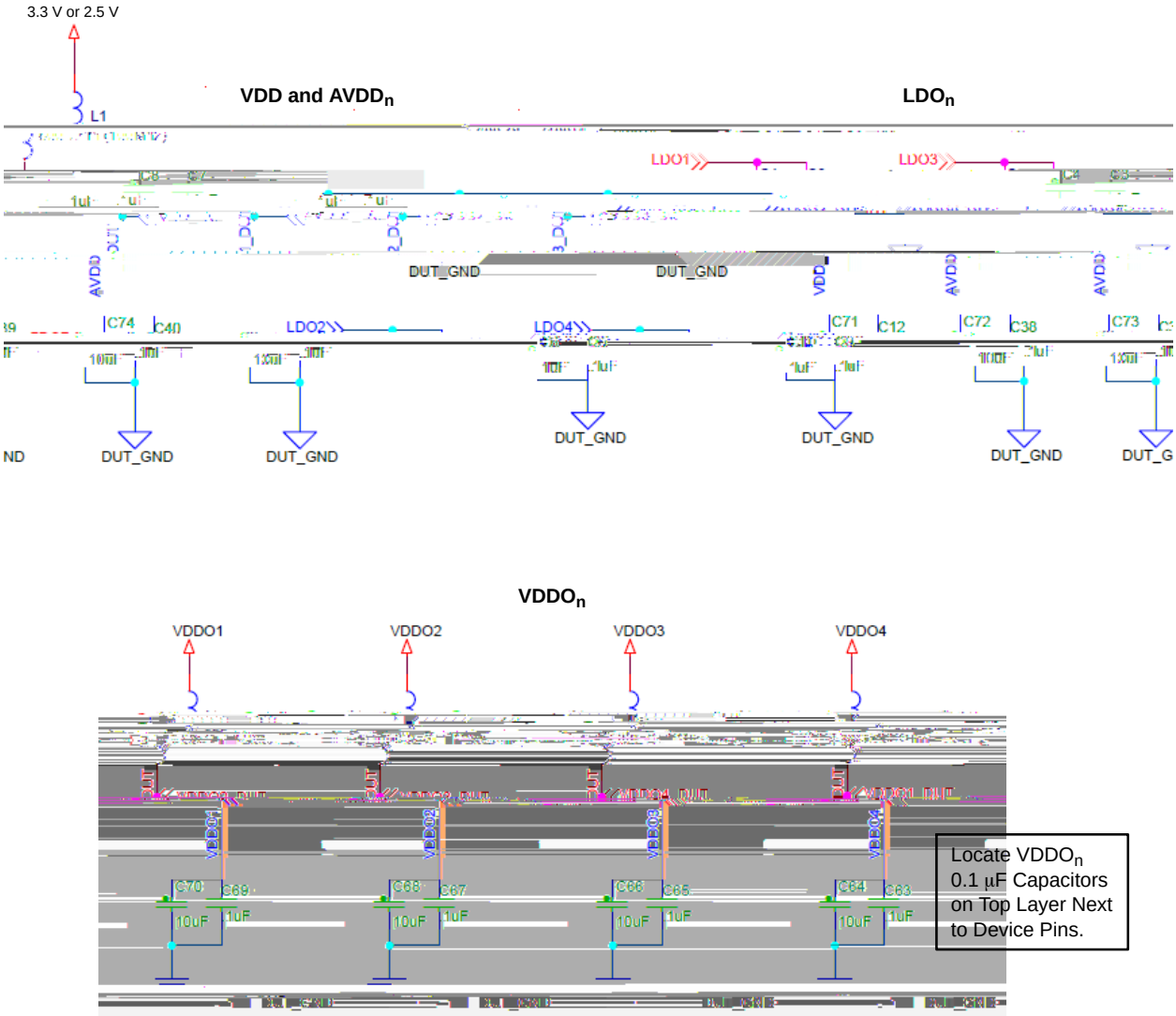


Figure 8. NB3H5150 Power Supply Filter Schemes

Table 10. RECOMMENDED CRYSTAL SPECIFICATIONS

Crystal	Fundamental AT−Cut
Frequency	25 MHz
Load Capacitance	16 pF − 20 pF
Shunt Capacitance, C0	7 pF Max
Equivalent Series Resistance	50 Ω Max
Initial Accuracy at 25°C	± 20 ppm
Temperature Stability	± 30 ppm
Aging	± 20 ppm
C0/C1 Ratio	250 Max
Crystal max Drive Level	100 μW

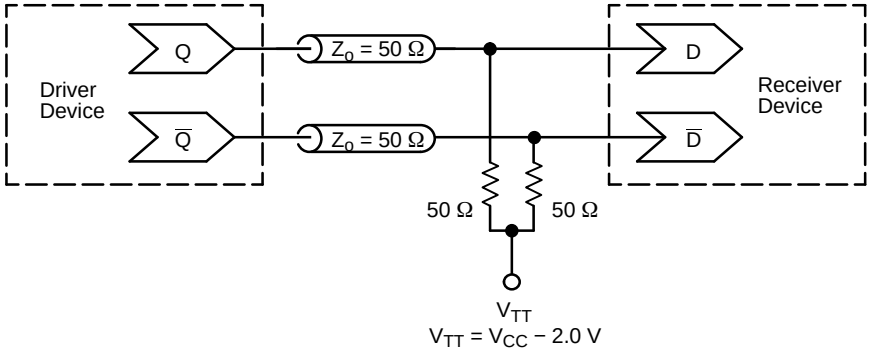


Figure 9. Typical Termination for LVPECL Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

Figure 10. Optional LVPECL output Loading and Termination

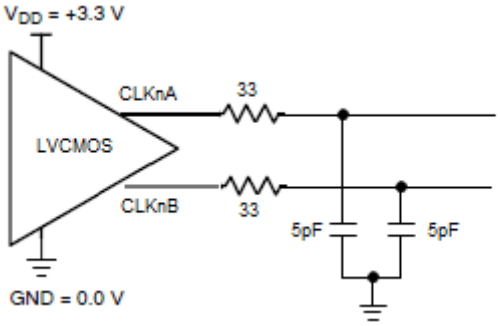


Figure 11. Typical LVCMOS Output Test Setup for Evaluation

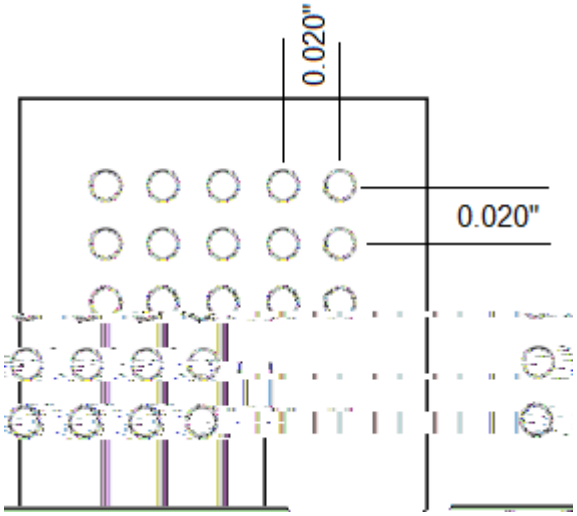


Figure 20. Via Layout Recommendation for Exposed Pad, QFN−32 Package

The exposed pad on the NB3H5150 QFN−32 package carries all of the power supply return currents. It is therefore important that the necessary current capability be satisfied, as well as the thermal transfer from the die to the PCB. Figure 20 shows a recommended via layout pattern for the exposed pad. Via spacing = 0.02”, filled vias preferred.

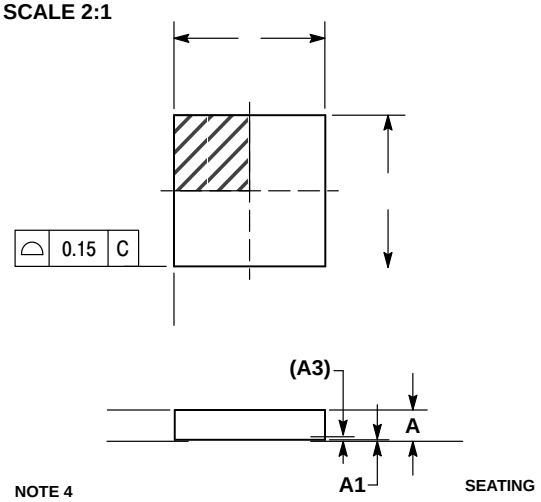
ORDERING INFORMATION

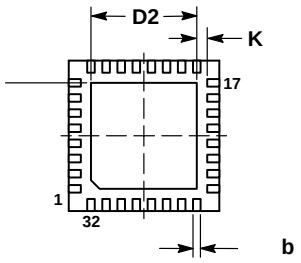
Device	Marking	Tables	Package	Shipping

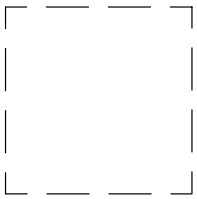
QFN32 5x5, 0.5P
CASE 485CE
ISSUE O

DATE 07 FEB 2012

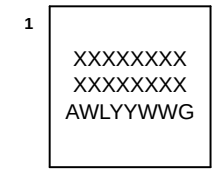
SCALE 2:1







GENERIC
MARKING DIAGRAM*



XXXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package