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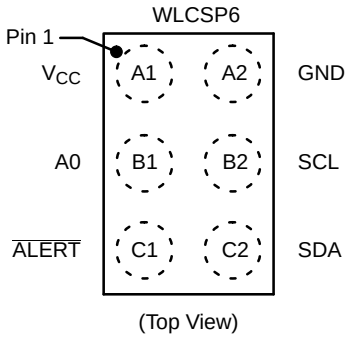
PIN CONFIGURATION



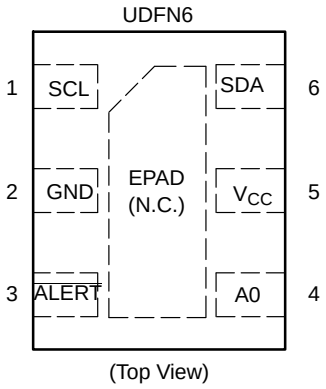


Table 2. PIN DESCRIPTIONS

Pin Name	Ball Number (WLCSP6)	Pin Number (UDFN6)	Description
A0	B1	4	Address selection pin
$\overline{\text{ALERT}}$	C1	3	Alert output pin
GND	A2	2	Ground
SCL	B2	1	Input clock pin
SDA	C2	6	Input/output data pin
VCC	A1	5	

Table 4. D.C. OPERATING CHARACTERISTICS (V_{CC} = 1.8 V, T_A = 25°C, unless otherwise specified)

Parameter		Conditions	Min	Typ	Max	Unit
TEMPERATURE INPUT						
Range			–40		+125	°C
Accuracy (Temperature Error)		–20°C to +85°C		±0.15	±0.75	°C
		–40°C to +125°C		±0.3	±1	°C
Accuracy vs. Supply				±0.03	±0.3	°C/V
DIGITAL INPUT/OUTPUT						
V_{IH}	Input Logic High Level		0.7 (VCC)		VCC	V
V_{IL}	Input Logic Low Level		–0.5		0.3 (VCC)	V
I_{IN}	Input Current	0 V < V_{IN} < (VCC) +0.3 V			1	μA
V_{OL}	Output Logic Low Level	VCC > 2 V, I_{OUT} = 3 mA			0.4	V
		VCC < 2 V, I_{OUT} = 3 mA			0.2 (VCC)	V
$\overline{ALERT}$ Internal Pull-up Resistor		$\overline{ALERT}$ to VCC	80	100	120	kΩ
Resolution				12		Bit
Conversion Time		One-Shot mode	17	22	28	ms
Conversion Modes		CR1 = 0, CR0 = 0		0.25		Conv/s
		CR1 = 0, CR0 = 1 (default)		1		Conv/s
		CR1 = 1, CR0 = 0		4		Conv/s
		CR1 = 1, CR0 = 1		16		Conv/s
Timeout Time			21	30	35	ms
POWER SUPPLY						
Operating Supply Range, VCC Pin			1.4		3.6	V
I_Q	Quiescent Current	Serial bus inactive, CR1 = 0, CR0 = 1 (default)		3.1	3.6	μA
		Serial bus inactive, CR1 = 0, CR0 = 1 (default), –40°C to +125°C		6		μA
		Serial bus active, SCL frequency = 400 kHz, CR1 = 0, CR0 = 1 (default)		8		μA
		Serial bus active, SCL frequency = 3.4 MHz, CR1 = 0, CR0 = 1 (default)		41		μA
I_{SD}	Shutdown Current	Serial bus inactive		2.5	3.1	μA
		Serial bus active, SCL frequency = 400 kHz		8		μA
		Serial bus active, SCL frequency = 3.4 MHz		41		μA
TEMPERATURE						
Specified Range			–40		+125	°C
Storage Range			–55		+150	°C

N34TS108

POINTER REGISTER

Figure 4 shows the internal register structure of the N34TS108. Use the 8-bit pointer register to address a given data register. The pointer register uses the two LSBs (see Table 16) to identify which of the data registers respond to a read or write command. Table 7 identifies the bits of the pointer register byte. Table 8 describes the pointer address of the registers available in the N34TS108. The power-up reset value of the P1 and P0 bits is ‘00’.

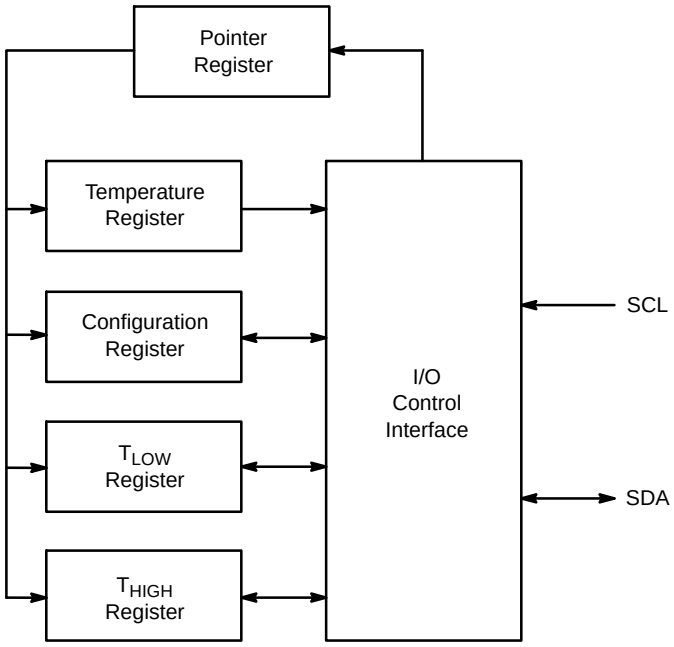


Figure 4. Internal Register Structure

Table 7. POINTER REGISTER BYTE

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	

Table 8. POINTER ADDRESSES

P1	P0	Register
0	0	Temperature Register (Read Only, Default)
0	1	Configuration Register (Read/write)
1	0	T_{LOW} Register (Read/Write)
1	1	T_{HIGH} Register (Read/Write)

TEMPERATURE REGISTER

The temperature register is configured as a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data, as shown in Table 9 and Table 10. Note that byte 1 is the most significant byte, followed by byte 2, the least significant byte. The first 12 bits are used to indicate temperature. There is no requirement to read the least significant byte if that information is not needed (for example, for resolution lower than 1°C). Table 11 summarizes the temperature data format. One LSB equals 0.0625°C. Negative numbers are represented in binary twos complement format. Following power-up or reset, the temperature register reads 0°C until the first conversion is complete. The unused bits in the temperature register always read '0'.

Table 9. BYTE 1 OF TEMPERATURE REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
T11	T10	T9	T8	T7	T6	T5	T4

Table 10. BYTE 2 OF TEMPERATURE REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
T3	T2	T1	T0	0	0	0	0

Table 11. TEMPERATURE DATA FORMAT (Note 4)

Temperature (°C)	Digital Output	
	Binary	Hex
128	0111 1111 1111	7FF
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
–0.25	1111 1111 1100	FFC
–25	1110 0111 0000	E70
–55	1100 1001 0000	C90

4. The temperature sensor ADC resolution is 0.0625°C/count.

Table 11 does not supply a full list of all temperatures. Use the following rules to obtain the digital data format for a given temperature.

●

CONFIGURATION REGISTER

The configuration register is a 16-bit read and write register used to store bits that control the operational modes of the temperature sensor. Read and write operations are performed MSB first. The format and power-up (reset) default value of the configuration register is shown in Table 12, followed by an explanation of the register bits.

Table 12. CONFIGURATION AND POWER-UP/RESET FORMAT

Byte	D7	D6	D5	D4	D3	D2	D1	D0
1	ID	CR1	CR0	FH	FL	TM	M1	M0
	0	0	1	0	0	1	1	0
2	POL	0	HYS1	HYS0	0	0	0	0
	0	0	0	1	0	0	0	0

Hysteresis Control (HYS1 and HYS0)

When operating in comparator mode, the hysteresis control bits (HYS1 and HYS0) configure the hysteresis for the limit comparison of the N34TS108 to 0°C, 1°C, 2°C, or 4°C. The default hysteresis is 1°C. Table 13 shows the settings for HYS1 and HYS0.

Table 13. HYSTERESIS SETTINGS

HYS1	HYS2	Hysteresis
0	0	0°C
0	1	1°C (Default)
1	0	2°C
1	1	4°C

Polarity (POL)

The polarity of the $\overline{\text{ALERT}}$ pin can be programmed using the POL bit. If POL = ‘0’ (default), the $\overline{\text{ALERT}}$ is active low. For POL = ‘1’, the $\overline{\text{ALERT}}$ pin is active high, and the state of the $\overline{\text{ALERT}}$ pin is inverted.

Mode Bits (M1 and M0)

The mode bits, M1 and M0, can be set to three dif63.1. 8 303.2504 4TD-.0022 Tc-.0002 Tw09For POL = ‘1’, t -1The bits, 0 0 0020, 0

Temperature Watchdog Flags (FL and FH)

The N34TS108 uses temperature watchdog flags in the configuration register that indicate the result of comparing the device temperature at the end of every conversion to the values stored in the temperature limit registers (T_{HIGH} and T_{LOW}). If the temperature of the N34TS108 exceeds the value in the T_{HIGH} register, then the flag-high bit (FH) in the configuration register is set to '1'. If the temperature falls below the value in the T_{LOW} register, then the flag-low bit (FL) is set to '1'. If both flag bits remain '0', then the temperature is within the temperature range set by the temperature limit registers. In interrupt mode, when any of the flags is set by an under- or over-temperature event, the SMBus $\overline{\text{ALERT}}$ Response only clears the pin and not the flags. Reading the configuration register clears both the flags and the pin unless the device is in comparator mode.

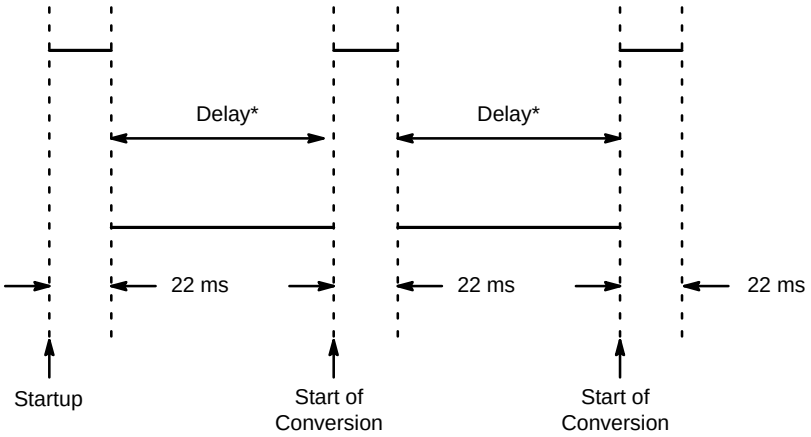
Conversion Rate

The conversion rate bits, CR1 and CR0, configure the N34TS108 for conversion rates of 0.25 Hz, 1 Hz, 4 Hz, or 16 Hz. The default rate is 1 Hz. The N34TS108 has a typical conversion time of 22 ms. To achieve different conversion rates, the N34TS108 makes a conversion, and then powers down and waits for the appropriate delay set by CR1 and CR0. Table 14 shows the settings for CR1 and CR0.

Table 14. CONVERSION RATE SETTINGS

CR1	CR0	Conversion Rate	I_Q (Typ)
0	0	0.25 Hz	3 μA
0	1	1 Hz (Default)	4 μA
1	0	4 Hz	5 μA
1	1	16 Hz	13 μA

After power-up or a general-call reset, the N34TS108 immediately starts a conversion, as shown in Figure 5. The first result is available after 22 ms (typical). The active quiescent current during conversion is 27 μA (typical at +25°C). The quiescent current during delay is 2.5 μA (typical at +25°C).



*Delay is set by the CR1 and CR0 bits in the configuration register.

Figure 5. Conversion Start

HIGH- AND LOW-LIMIT REGISTERS

In comparator mode (TM = '0'), the $\overline{\text{ALERT}}$ pin becomes active when the temperature exceeds the value in the T_{HIGH} register or drops below the value in the T_{LOW} register. The $\overline{\text{ALERT}}$ pin remains active until the temperature returns to a value that is within the range set by:

$$(T_{LOW} + HYS) \text{ and } (T_{HIGH} - HYS) \qquad \text{(eq. 1)}$$

Where:

HYS is the hysteresis set by the hysteresis control bits (HYS1 and HYS0).

In interrupt mode (TM = '1'), the $\overline{\text{ALERT}}$ pin becomes active when the temperature exceeds the value in the T_{HIGH} register or drops below the value in the T_{LOW} register, and remains active until a read operation of the configuration register occurs (also clears the values latched in the watchdog flags, FL and FH), or the device successfully responds to the SMBus alert response address. The $\overline{\text{ALERT}}$ pin is also cleared by resetting the device with the general call reset command.

Both operational modes are represented in Figure 6 and Figure 7.

Table 15 and Table 16 describe the format for the T_{HIGH} and T_{LOW} registers. Note that the most significant byte is sent first, followed by the least significant byte. Power-up (reset) default values are T_{HIGH} = +127.9375°C and T_{LOW} = –128°C. These values ensure that upon power-up, the limit window is set to maximum, and the $\overline{\text{ALERT}}$ pin does not become active until the desired limit values are programmed in the registers. Other default values for the temperature limits are available by request. The format of the data for T_{HIGH} and T_{LOW} is the same as for the temperature register.

Table 15. BYTES 1 AND 2 OF T_{HIGH} REGISTER

Byte	D7	D6	D5	D4	D3	D2	D1	D0
1	H11	H10	H9	H8	H7	H6	H5	H4

Byte	D7	D6	D5	D4	D3	D2	D1	D0
2	H3	H2						

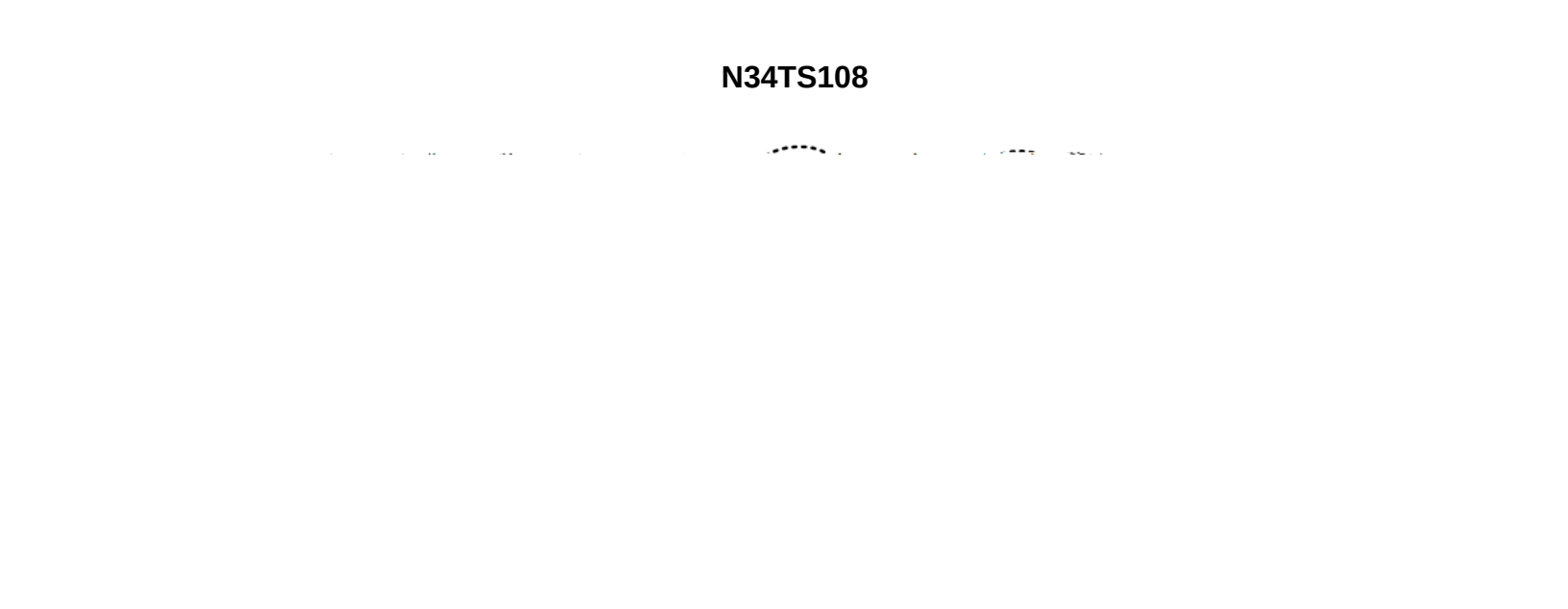


Figure 7. Comparator Mode

SERIAL INTERFACE

The N34TS108 operates as a slave device only on the two-wire bus and SMBus. Connections to the bus are made using the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The N34TS108 supports the transmission protocol for both fast (1 kHz to 400 kHz) and high-speed (1 kHz to 3.4 MHz) modes. All data bytes are transmitted MSB first.

SERIAL BUS ADDRESS

To communicate with the N34TS108, the master must first communicate with slave devices using a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing either a read or write operation. The N34TS108 features an address pin that allows up to three devices to be addressed on a single bus. The N34TS108 latches the status of the address pin at the start of a communication. Table 17 describes the pin logic levels and the corresponding address values. Other values for the fixed address bits are available by request.

Table 17. ADDRESS PIN AND SLAVE ADDRESSES

Device Two-wire Address

data are required. The master can then generate a start condition and send the slave address byte with the R/W bit high to initiate the read command. If repeated reads from the same register are desired, it is not necessary to continually send the pointer register bytes because the N34TS108 stores the pointer register value until it is changed by the next write operation.

Note that register bytes are sent with the most significant

Table 18. ORDERING INFORMATION

Device Order Number	Marking	Package Type	Temperature Range	Pin 1 Quadrant (See Below)	Shipping†
N34TS108C6ECT5G	C	WLCSP 6-ball	−40°C to +125°C	1	5,000 / Tape & Reel
N34TS108MUET3G	A	UDFN 6	− 40°C to +125°C	2	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

5. All packages are RoHS-compliant (Lead-free Halogen-free).
6. The standard lead/ball finish is SnAgCu.

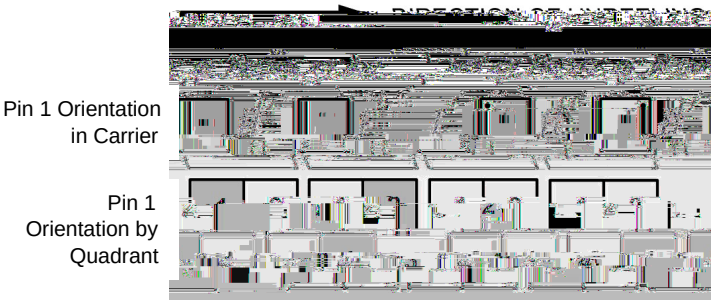


Figure 8. Pin 1 Orientation in Tape and Reel

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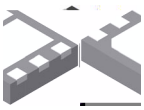

UDFN6 2x2, 0.65P
CASE 517DR
ISSUE A

DATE 25 JAN 2022

X = Specific Device Code
M = Date Code
▪

WLCSP6, 1.1888x0.788x0.625
CASE 567YQ
ISSUE O

DATE 12 NOV 2019

GENERIC