N25S830HA

256 b L P S a SRAM

32 k x 8 Bit Organization

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Introduction

The ON Semiconductor serial SRAM family includes several integrated memory devices including this 256 kb serially accessed Static Random Access Memory, internally organized as 32 k words by 8 bits. The devices are designed and fabricated using ON Semiconductor's advanced CMOS technology to provide both high−speed performance and low power. The devices operate with a single chip select ($\overline{CS}$) input and use a simple Serial Peripheral Interface (SPI) serial bus. A single data in and data out line is used along with a clock to access data within the devices. The N25S830HA devices include a $\overline{HOLD}$ pin that allows communication to the device to be paused. While paused, input transitions will be ignored. The devices can operate over a wide temperature range of −40°C to +85°C and can be available in several standard package offerings.

Features

- **Power Supply Range:** 2.7 to 3.6 V
- **Very Low Standby Current:** Typical Isb as low as 1 □A
- **Very Low Operating Current:** As low as 3 mA
- **Simple Memory Control:**
  Single chip select ($\overline{CS}$)
  Serial input (SI) and serial output (SO)
- **Flexible Operating Modes:**
  Word read and write
  Page mode (32 word page)
  Burst mode (full array)
- **Organization:** 32 K x 8 bit
- **Self Timed Write Cycles**
- **Built−in Write Protection ($\overline{CS}$ High)**
- **$\overline{HOLD}$ Pin for Pausing Communication**
- **High Reliability:** Unlimited write cycles
- Green SOIC and TSSOP
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

ORDERING INFORMATION

Device	Package	
N25S830HAS22I	SOIC−8 (Pb−Free)	

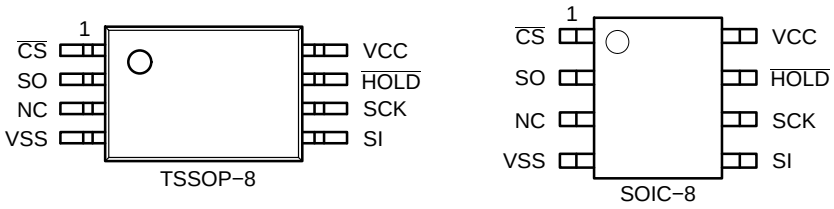


Figure 1. Pin Connections
(Top View)

Table 1. DEVICE OPTIONS

Part Number	Density	Power Supply (V)	Speed (MHz)	Package	Typical Standby Current	Read/Write Operating Current
N25S830HAS2	256 Kb	3.0	20	SOIC	1 □A	3 mA @ 1 Mhz
N25S830HAT2				TSSOP		

Table 2. PIN NAMES

Pin Name	Pin Function
$\overline{CS}$	Chip Select Input
SCK	Serial Clock Input
SI	Serial Data Input
SO	Serial Data Output
$\overline{HOLD}$	Hold Input
NC	No Connect
V_{CC}	Power
V_{SS}	Ground

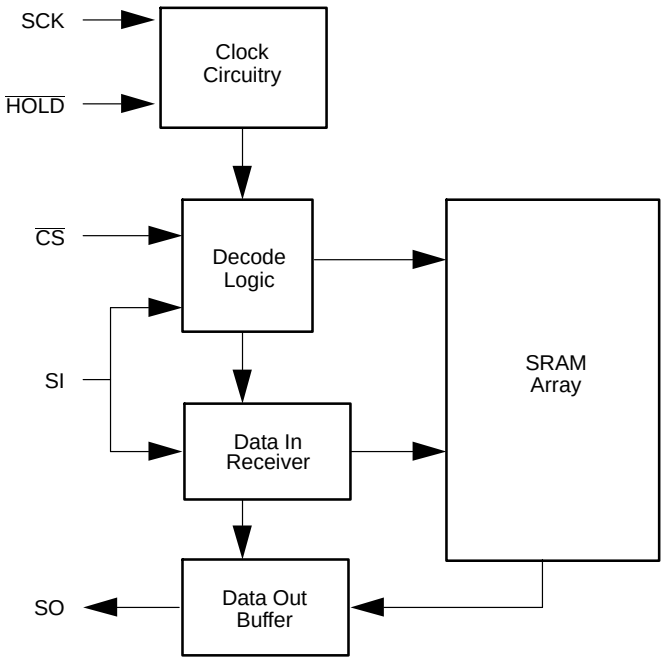
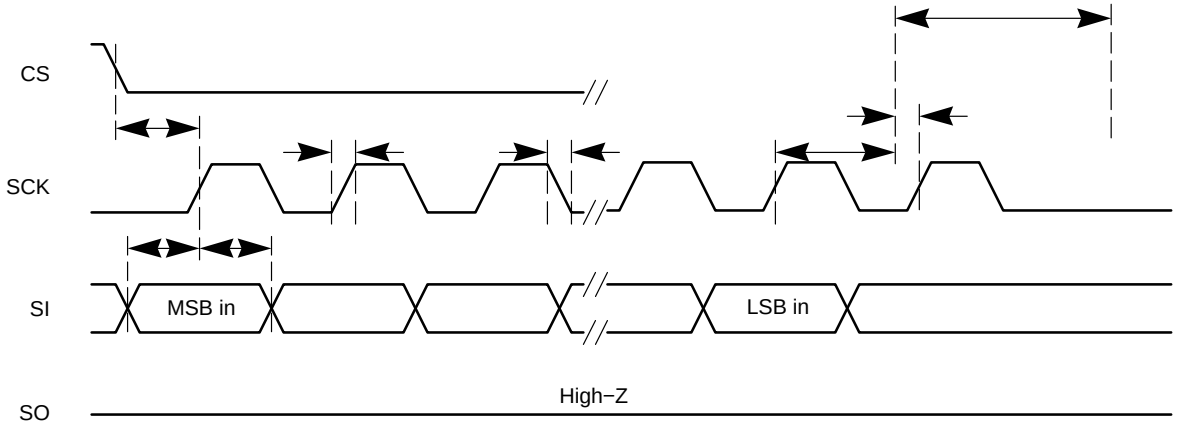
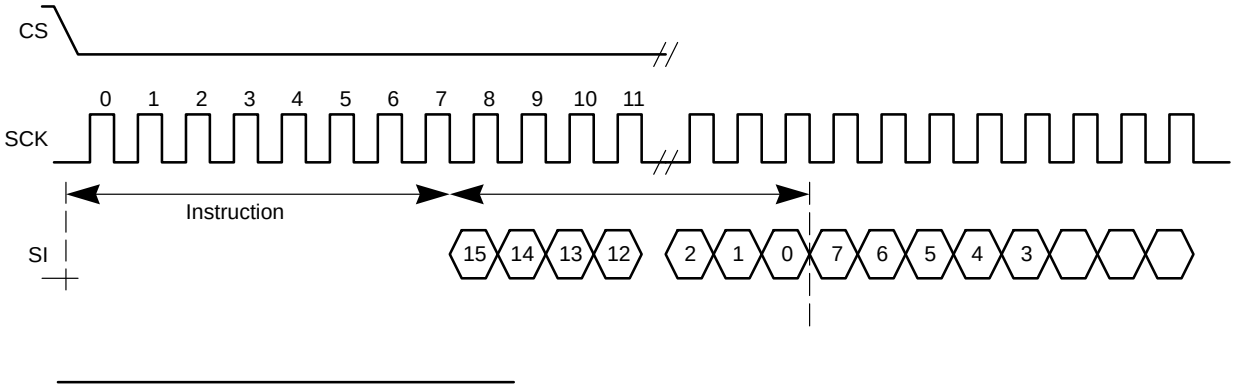


Figure 2. Functional Block Diagram

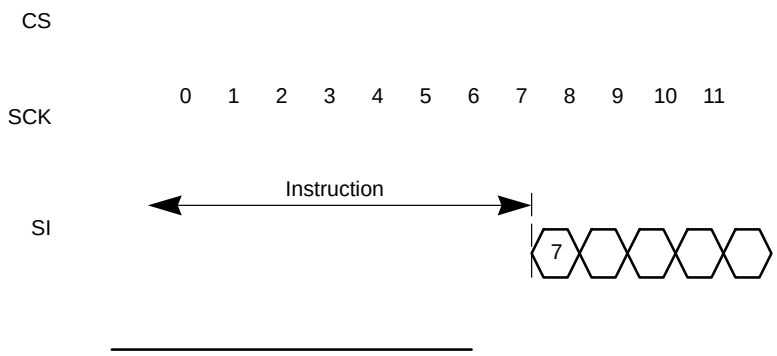
Table 3. ABSOLUTE MAXIMUM RATINGS


CS
SCK
SI
MSB in
LSB in
SO
High−Z


CS
SCK
0 1 2 3 4 5 6 7 8 9 10 11
Instruction
SI
15 14 13 12
2 1 0 7 6 5 4 3

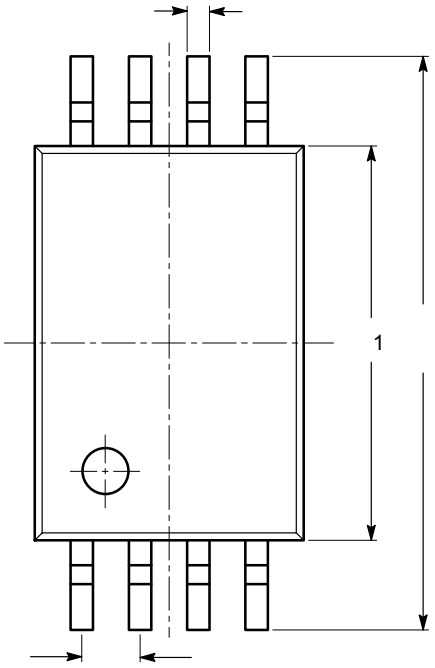
WRITE Status Register Instruction (WRSR)

This instruction provides the ability to write the status register and select among several operating modes. Several of the register bits must be set to a low ‘0’ if any of the other bits are written. The timing sequence to write to the status register is shown below, followed by the organization of the status register.



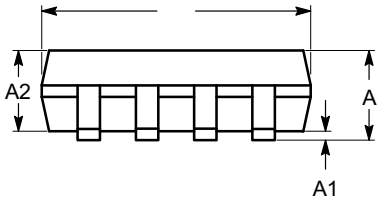
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

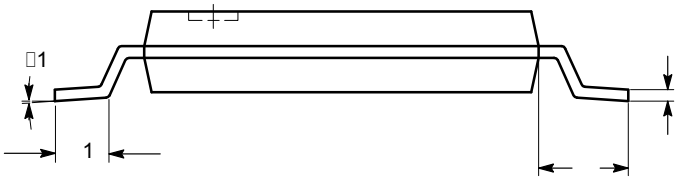


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0		8



SIDE VIEW



END VIEW

Notes:
(1) A a . A .
(2) h -153.

PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O