

N25S818HA

256 kb L P e S e i a l SRAM

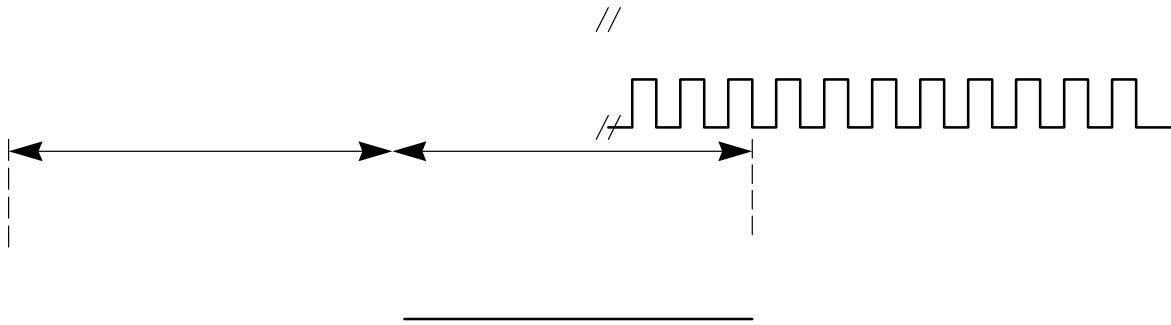
32 k x 8 Bit Organization

Introduction

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Table 8. CONTROL SIGNAL DESCRIPTIONS

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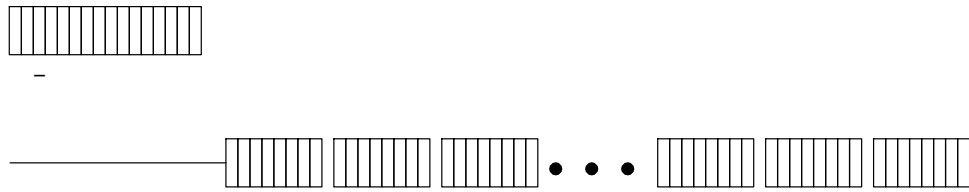


Figure 8. Page READ Sequence

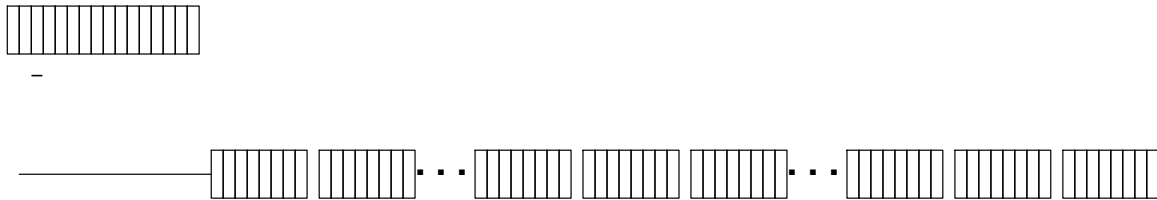


Figure 9. Burst READ Sequence

WRITE Operations

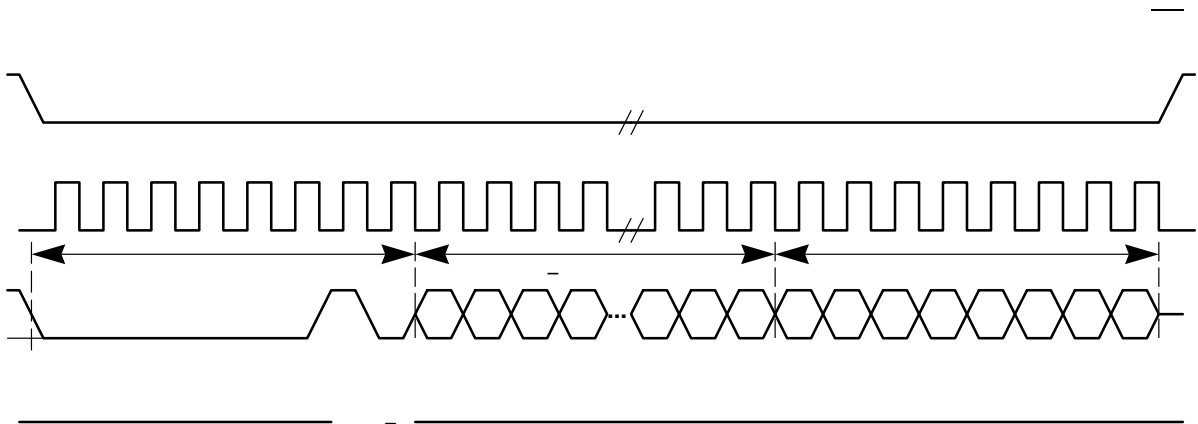
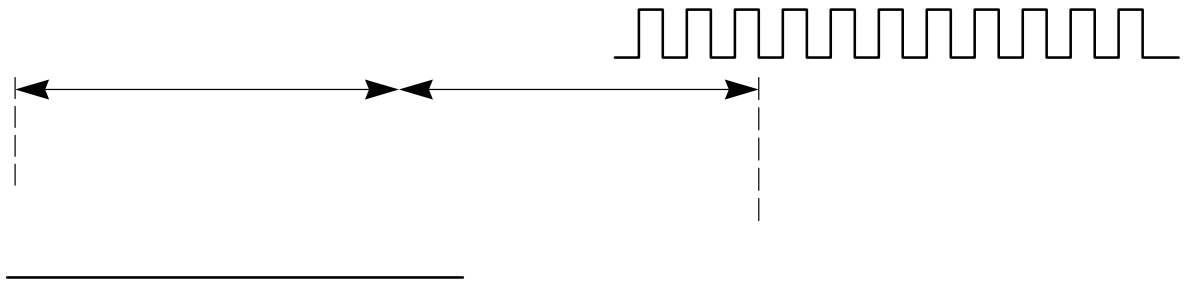


Figure 10. Word WRITE Sequence

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WRITE Status Register Instruction (WRSR)

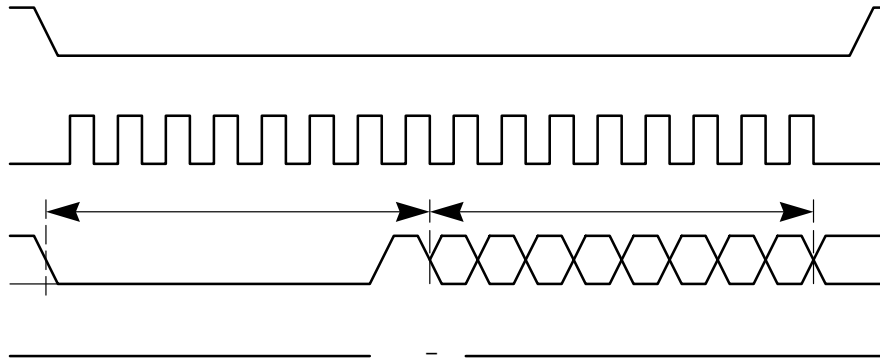


Figure 14. WRITE Status Register Sequence

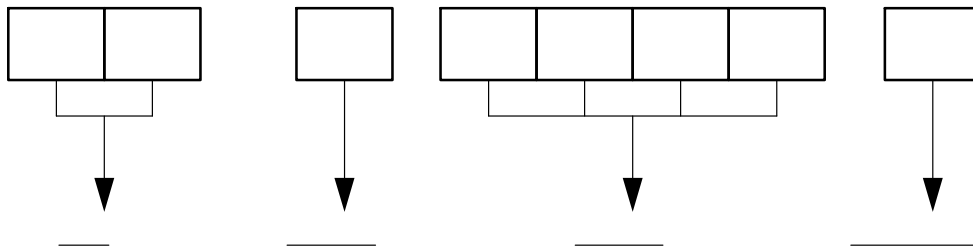
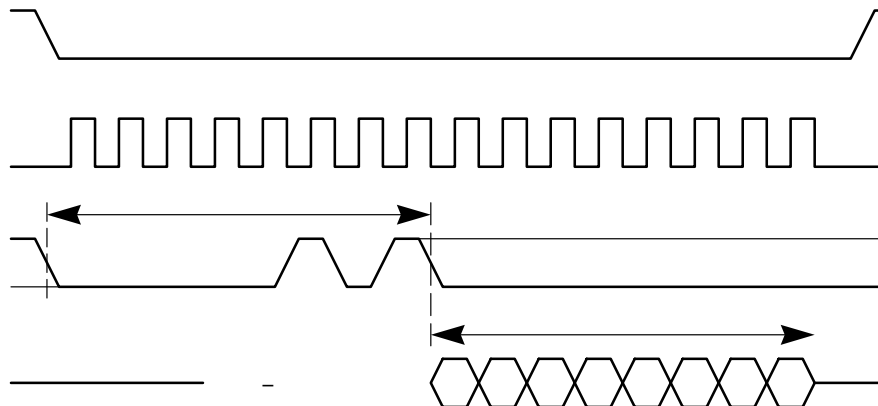


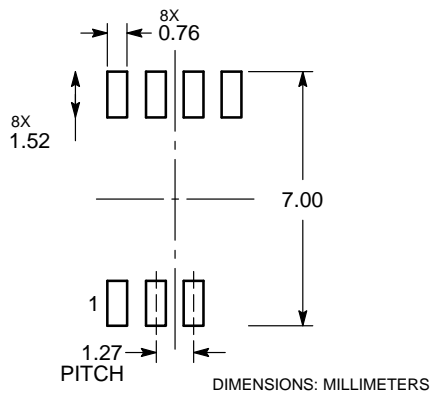
Figure 15. Status Register

READ Status Register Instruction (RDSR)



SOIC-8
CASE 751AZ
ISSUE B

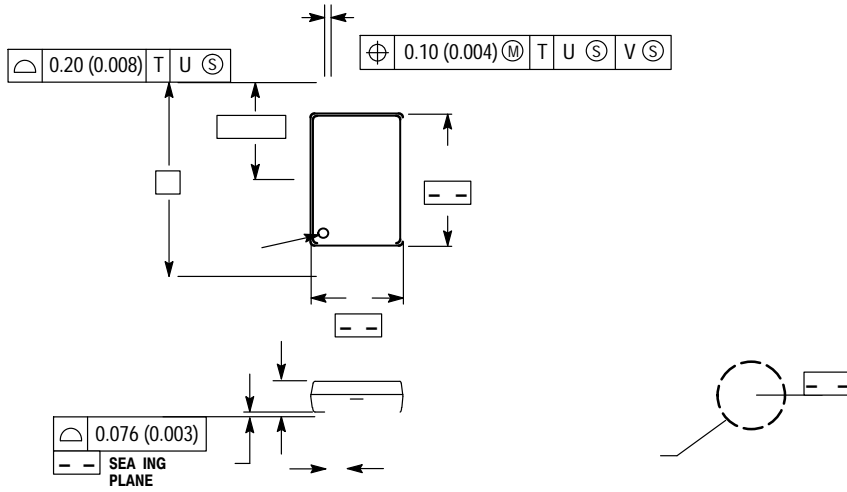
DATE 18 MAY 2015



*For

CASE 948S
ISSUE C

DATE 20 JUN 2008

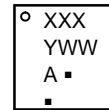


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MA	MIN	MA
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026 BSC	

L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°



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