N01S818HA

1 Mb Ultra−Low Power Serial SRAM

Standard SPI Interface and Multiplex DUAL and QUAD Interface

Overview

The ON Semiconductor serial SRAM family includes several integrated memory devices including this 1 Mb serially accessed Static Random Access Memory, internally organized as 128 K words by 8 bits. The devices are designed and fabricated using ON Semiconductor's advanced CMOS technology to provide both high-speed performance and low power. The devices operate with a single chip select ($\overline{CS}$) input and use a simple Serial Peripheral Interface (SPI) protocol. In SPI mode, a single data-in (SI) and data-out (SO) line is used along with the clock (SCK) to access data within the device. In DUAL mode, two multiplexed data-in/data-out (SIO0-SIO1) lines are used and in QUAD mode, four multiplexed data-in/data-out (SIO0-SIO3) lines are used with the clock to access the memory.

The devices can operate over a wide temperature range of −40

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Write Operation

The serial SRAM WRITE is selected by enabling $\overline{CS}$ low. First, the 8-bit WRITE instruction is transmitted to the device followed by the 24-bit address with the 7 MSBs being don't care. After the WRITE instruction and addresses are sent, the data to be stored in memory is shifted in on the SI pin.

If operating in page mode, after the initial word of data is shifted in, additional data words can be written as long as the address requested is sequential on the same page. Simply write the data on SI pin and continue to provide clock pulses. The internal address pointer is automatically incremented to the next higher address on the page after each word of data is written in. This can be continued for the entire page length of 32 words long. At the end of the page, the addresses pointer will be wrapped to the 0 word address within the page and the operation can be continuously looped over the 32 words of the same page. The new data will replace data already stored in the memory locations.

If operating in burst mode, after the initial word of data is shifted in, additional data words can be written to the next sequential memory locations by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each word of data is read out. This can be continued for the entire array and when the highest address is reached, 1FFFFh, the address counter wraps to the address 00000h. This allows the burst write cycle to be continued indefinitely. Again, the new data will replace data already stored in the memory locations.

All WRITE operations are terminated by pulling $\overline{CS}$ high.

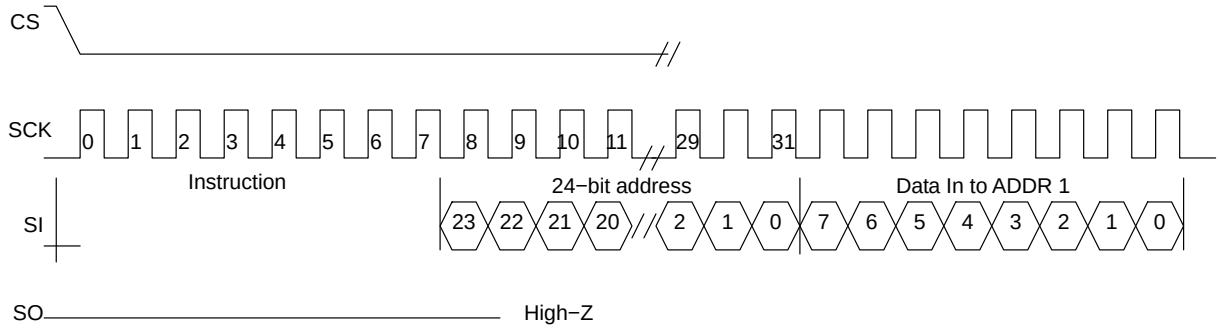
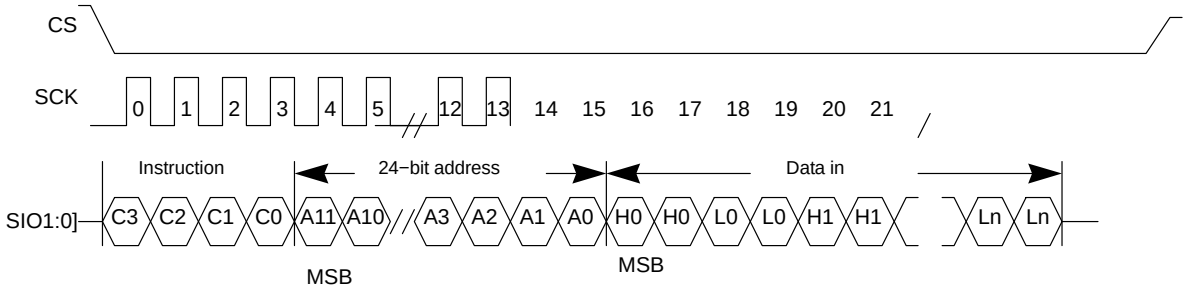
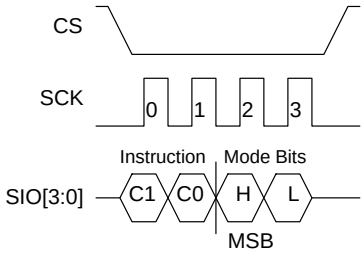


Figure 6. SPI Write Sequence



Notes:

Figure 7. DUAL Write Sequence



Notes: C[1:0] = 01h

Figure 14. QUAD Write Mode Register Sequence

Table 5. MODE REGISTER

Bit	Function
0	Hold Function 1 = Hold function disabled 0 = Hold function enabled (Default)
1	Reserved
2	Reserved
3	Reserved
4	Reserved
5	Reserved
6	Operating Mode Bit 7 Bit 6 0 0 = Word Mode 1 0 = Page Mode

Table 8. CAPACITANCE (Note 3)

Item	Symbol

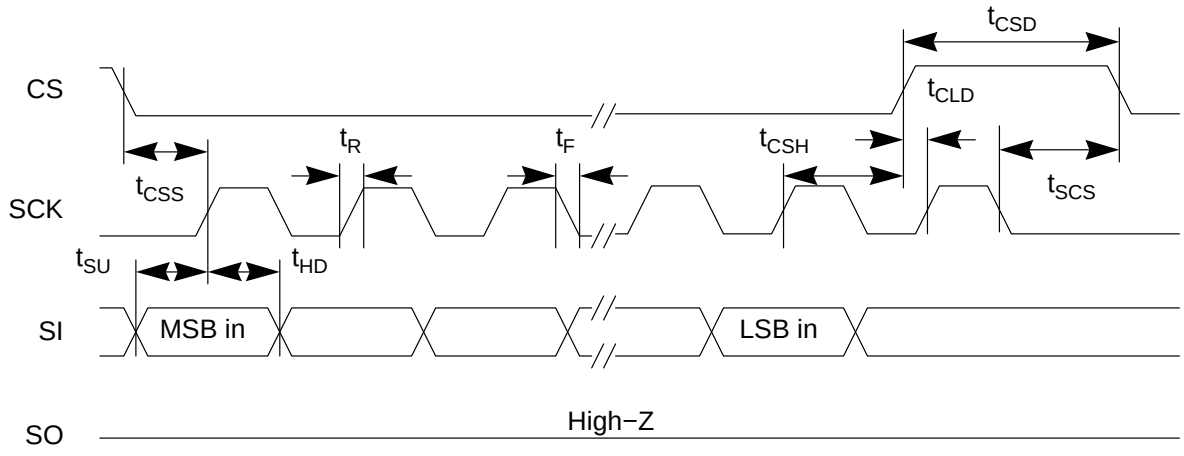


Figure 15. SPI Input Timing

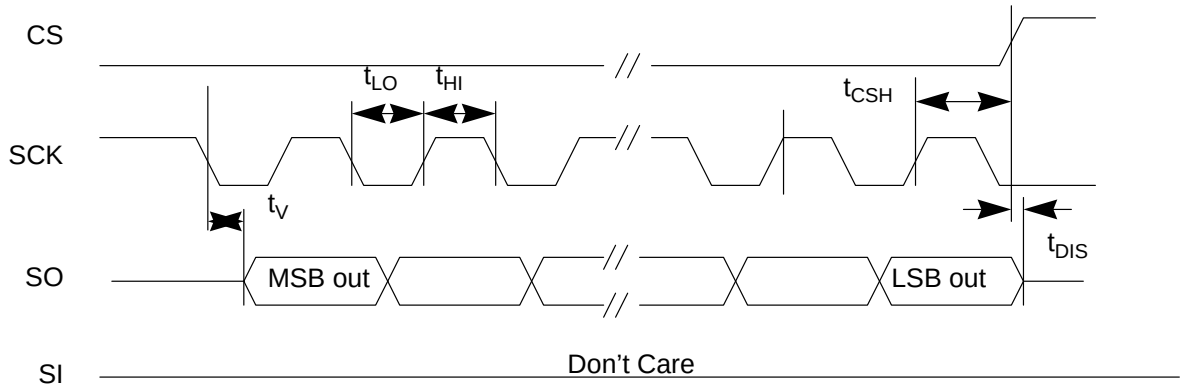


Figure 16. SPI Output Timing

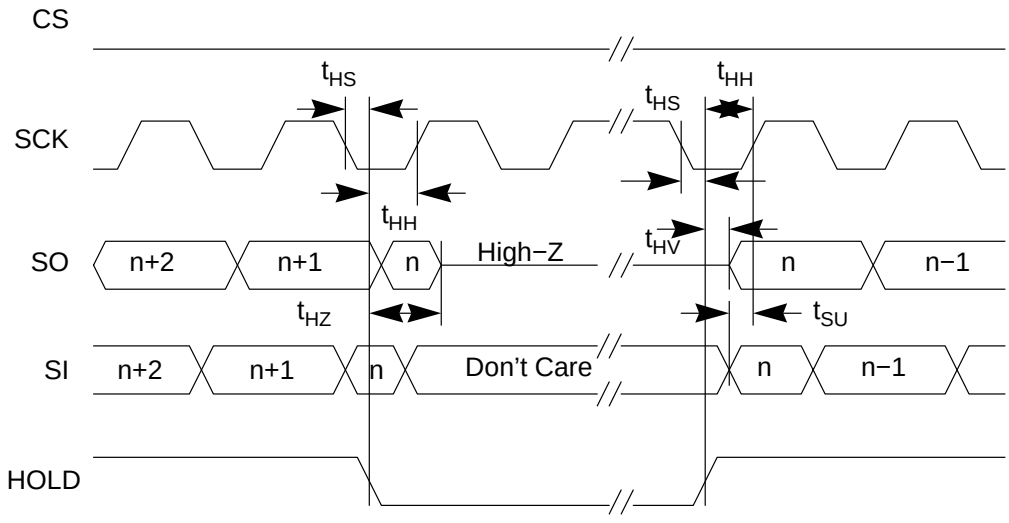


Figure 17. SPI Hold Timing

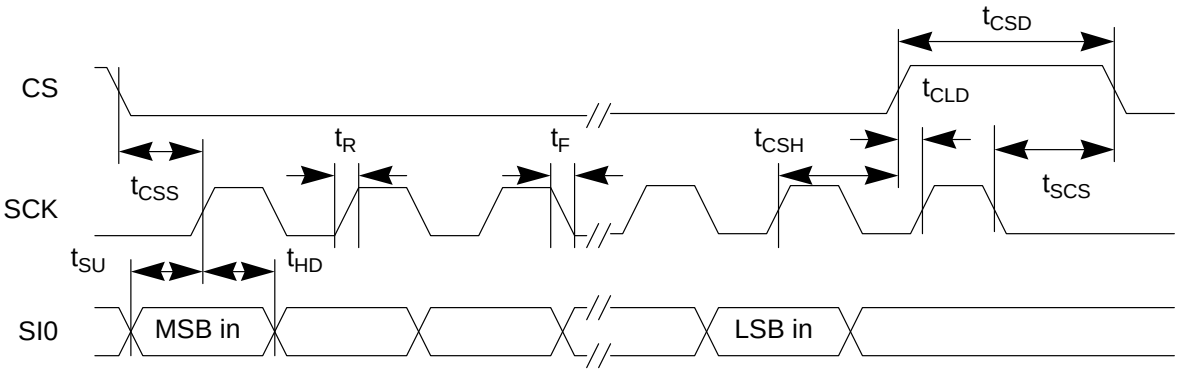


Figure 18. QUAD Input Timing

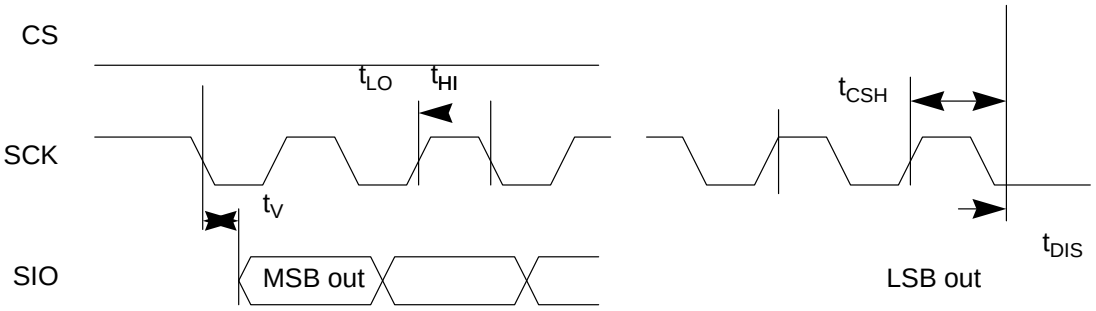


Figure 19. QUAD Output Timing

PACKAGE DIMENSIONS

TSSOP8 3x4.4 / TSSOP8 (225 mil)
CASE 948BH
ISSUE O