

MC74LVX4245

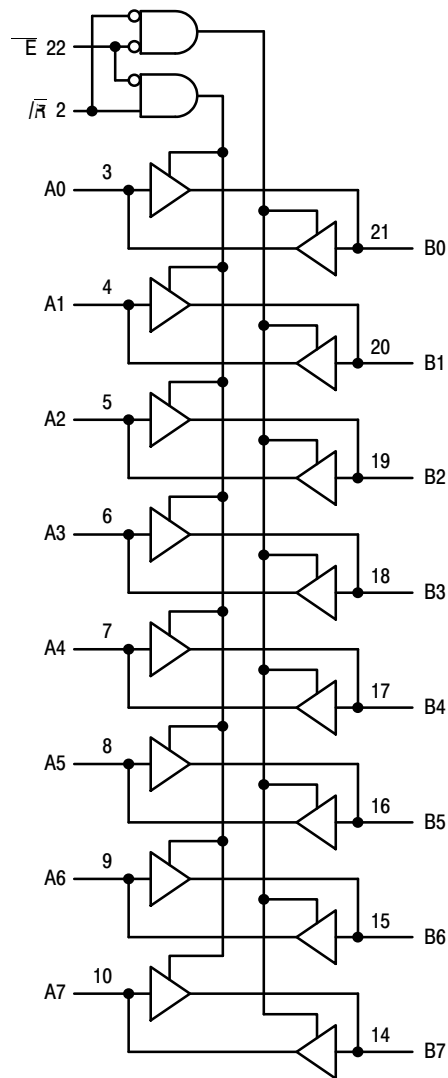


Figure 2. Logic Diagram

INPUTS		OPERATING MODE Non-Inverting
OE	T/R	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions are Acceptable; For I_{CC} reasons, Do Not Float Inputs

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V_{CCA}, V_{CCB}	DC Supply Voltage	-0.5 to +7.0		V
V_I	DC Input Voltage $\overline{OE}, T/\overline{R}$	-0.5 to $V_{CCA} + 0.5$		V
$V_{I/O}$	DC Input/Output Voltage	An	-0.5 to $V_{CCA} + 0.5$	V
		Bn	-0.5 to $V_{CCB} + 0.5$	V
I_{IK}	DC Input Diode Current $\overline{OE}, T/\overline{R}$	± 20	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	± 50	$V_O < GND; V_O > V_{CC}$	mA

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CCA}	V _{CCB}	T _A = 25°C		T _A = -40 to +85°C		Unit	
					Typ	Guaranteed Limits				
I _{IN}	Max Input Leakage Current	$\overline{OE}, T/\overline{R}$ V _I = V _{CCA} , GND	5.5	3.6		±0.1	±1.0		μA	
I _{OZA}	Max 3-State Output Leakage	A _n V _I = V _{IH} , V _{IL} $\overline{OE} = V_{CCA}$ V _O = V _{CCA} , GND	5.5	3.6		±0.5	±5.0		μA	
I _{OZB}	Max 3-State Output Leakage	B _n V _I = V _{IH} , V _{IL} $\overline{OE} = V_{CCA}$ V _O = V _{CCB} , GND	5.5	3.6		±0.5	±5.0		μA	
ΔI _{CC}	Maximum I _{CCT} per Input	A _n , \overline{OE} T/ \overline{R}	V _I = V _{CCA} - 2.1V	5.5	3.6	1.0	1.35	1.5		mA
		B _n	V _I = V _{CCB} - 0.6V	5.5	3.6		0.35	0.5		mA
I _{CCA}	Quiescent V _{CCA} Supply Current	A _n = V _{CCA} or GND B _n = V _{CCB} or GND $\overline{OE} = GND$ T/ $\overline{R} = GND$	5.5	3.6		8	80		μA	

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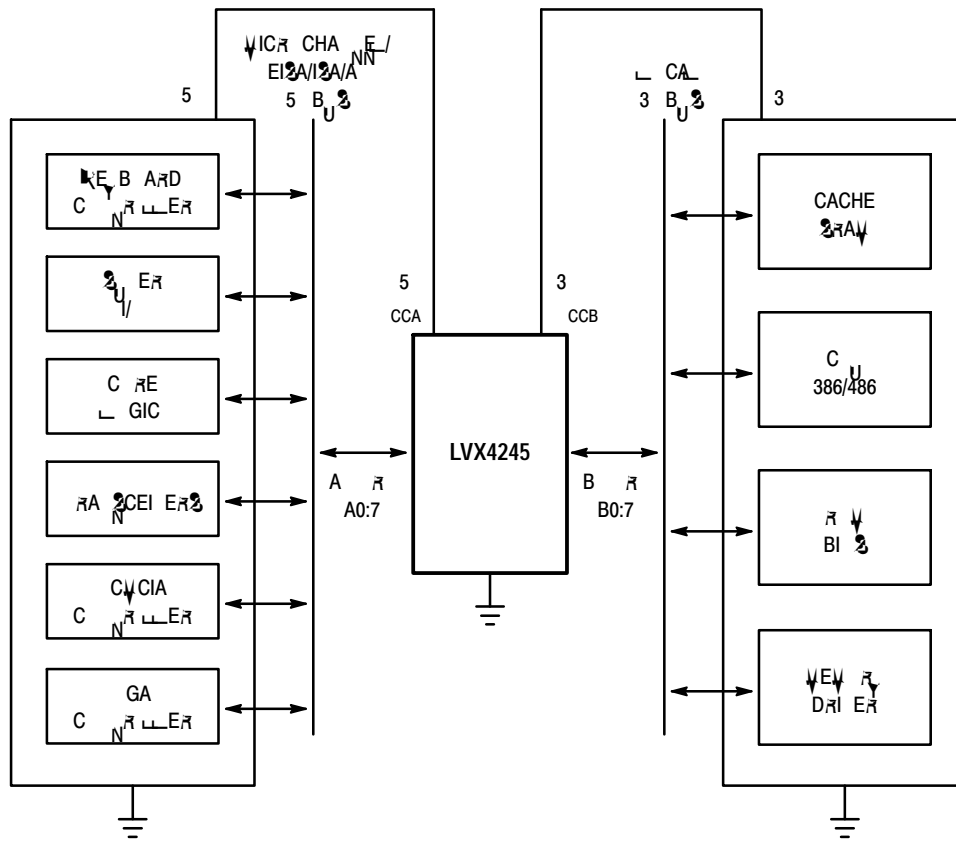


Figure 4. MC74LVX4245 Fits Into a System with 3V Subsystem and 5V Subsystem

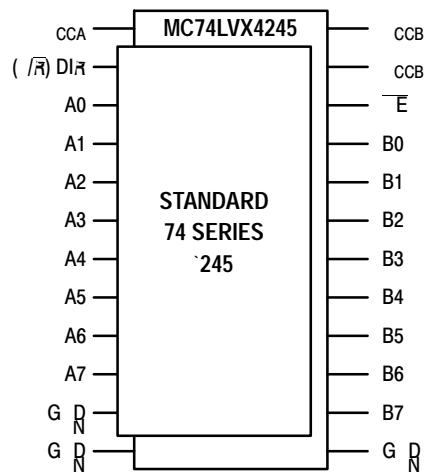
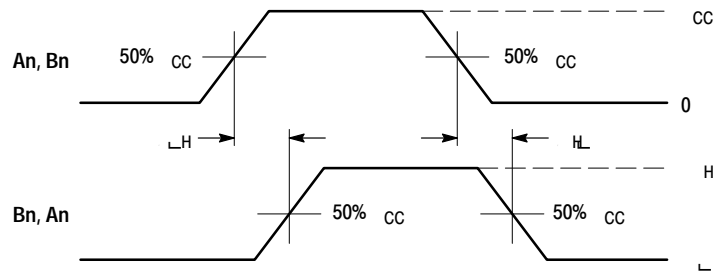
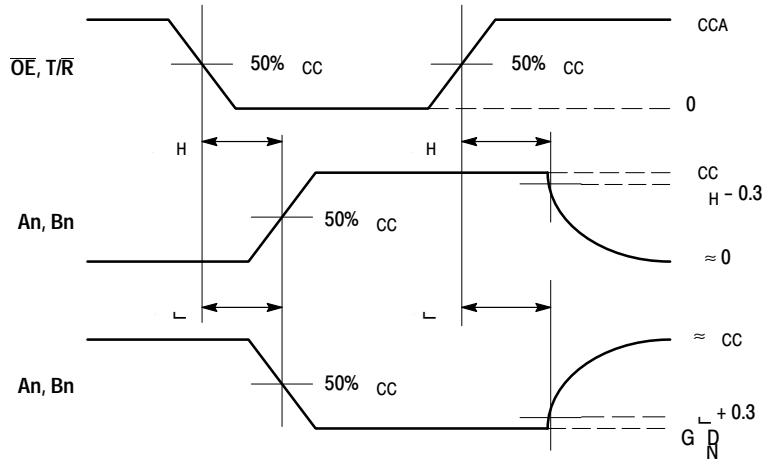


Figure 5. MC74LVX4245 Pin Arrangement Is Compatible to 20-Pin 74 Series '245s

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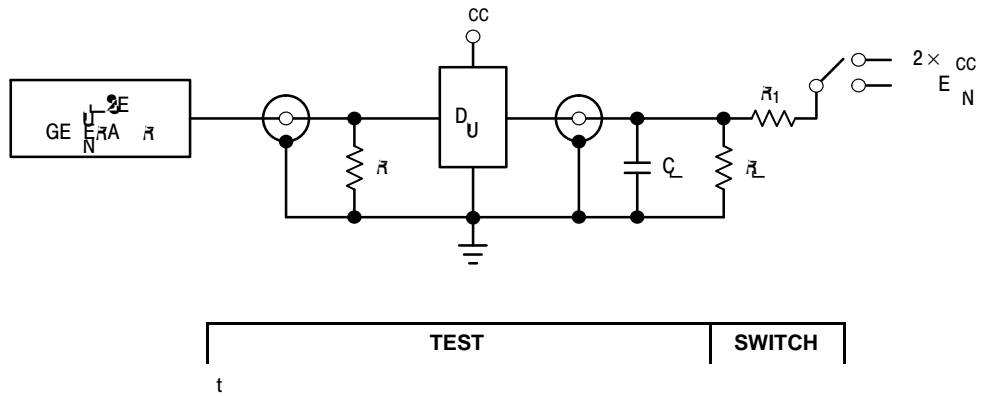


WAVEFORM 1 - PROPAGATION DELAYS
 $t_{LH} = t_{HL} = 2.5 \tau_{10\% \rightarrow 90\%} = 1 \mu H$; $t_{\text{prop}} = 500$



WAVEFORM 2 - OUTPUT ENABLE AND DISABLE TIMES
 $t_{H} = t_{L} = 2.5 \tau_{10\% \rightarrow 90\%} = 1 \mu H$; $t_{\text{prop}} = 500$

Figure 6. AC Waveforms



4/10/12

SOIC-24 WB
CASE 751E-04
ISSUE F

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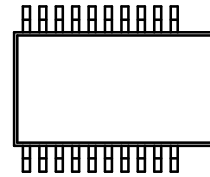


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.08 MAX AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	---	1.20
1	0.0	0.1
	0.1	0.0
	0.0	0.20
	.0	± 0

1	.0	.0
	0.	
	0.0	0.
2	0.2	
	0°	°



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