MC74HC4046B

Pha e-Locked Loop

High−Performance Silicon−Gate CMOS

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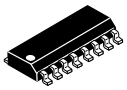

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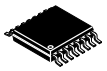
CASE 751B



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The MC74HC4046B is similar in function to the MC14046 Metal gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC4046B phase−locked loop contains three phase comparators, a voltage−controlled oscillator (VCO) and unity gain op−amp DEM_{OUT}. The comparators have two common signal inputs, $COMP_{IN}$, and SIG_{IN}. Input SIG_{IN} and $COMP_{IN}$ can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor to small voltage signals). The self−bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal $PC1_{OUT}$ and maintains 90 degrees phase shift at the center frequency between SIG_{IN} and $COMP_{IN}$ signals (both at 50% duty cycle). Phase comparator 2 (with leading−edge sensing logic) provides digital error signals $PC2_{OUT}$ and PCP_{OUT} and maintains a 0 degree phase shift between SIG_{IN} and $COMP_{IN}$ signals (duty cycle is immaterial). The linear VCO produces an output signal VCO_{OUT} whose frequency is determined by the voltage of input VCO_{IN} signal and the capacitor and resistors connected to pins C1A, C1B, R1 and R2. The unity gain op−amp output DEM_{OUT} with an external resistor is used where the VCO_{IN} signal is needed but no loading can be tolerated. The inhibit input, when high, disables the VCO and all op−amps to minimize standby power consumption.

Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage−to−frequency conversion and motor speed control.

Features

- Output Drive Capability: 10 LSTTL Loads
- Low Power Consumption Characteristic of CMOS Devices
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range for VCO: 3.0 to 6.0 V
- Low Input Current: 1.0 μA Maximum (except SIG_{IN} and $COMP_{IN}$)
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Low Quiescent Current: 80 μA Maximum (VCO disabled)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs
- Chip Complexity: 279 FETs or 70 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

MARKING DIAGRAMS