

The MC34025 series are high speed, fixed frequency, double-ended pulse width modulator controllers optimized for high frequency operation. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature an oscillator, a temperature compensated reference, a wide bandwidth error amplifier, a high speed current sensing comparator, steering flip-flop, and dual high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, and a latch for single pulse metering.

The flexibility of this series allows it to be easily configured for either current mode or voltage mode control.

#### **Features**

- 50 ns Propagation Delay to Outputs
- Dual High Current Totem Pole Outputs
- Wide Bandwidth Error Amplifier
- Fully-Latched Logic with Double Pulse Suppression
- Latching PWM for Cycle–By–Cycle Current Limiting
- Soft-Start Control with Latched Overcurrent Reset
- Input Undervoltage Lockout with Hysteresis
- Low Startup Current (500 μA Typ)
- Internally Trimmed Reference with Undervoltage Lockout
- 45% Maximum Duty Cycle (Externally Adjustable)
- Precision Trimmed Oscillator
- Voltage or Current Mode Operation to 1.0 MHz
- Functionally Similar to the UC3825
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

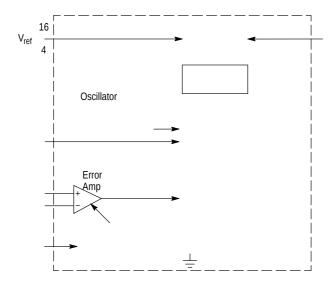


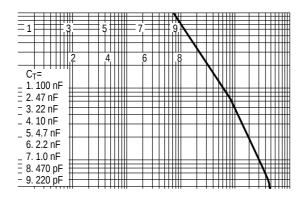
Figure 1. Simplified Application

#### **MAXIMUM RATINGS**

Rating	Symbol	Value	Unit	
Power Supply Voltage	Vcc	30	V	
Output Driver Supply Voltage	Vc	25	V	
Output Current, Source or Sink (Note 1) DC Pulsed (0.5 μs)	Io	0.5 2.0	А	
Current Sense, Soft–Start, Ramp, and Error Amp Inputs	V <sub>in</sub>	-0.3 to +7.0	V	
Error Amp Output and Soft-Start Sink Current	Io	10	mA	
Clock and R <sub>T</sub> Output Current	I <sub>co</sub>	5.0	mA	
Power Dissipation and Thermal Characteristics SO–16 Package (Case 751G) Maximum Power Dissipation @ T <sub>A</sub> = +25°C Thermal Resistance, Junction–to–Air DIP Package (Case 648) Maximum Power Dissipation @ T <sub>A</sub> = +25°C Thermal Resistance, Junction–to–Air	P <sub>D</sub> R <sub>θJA</sub> P <sub>D</sub> R <sub>θJA</sub>	862 145 1.25 100	mW °C/W W °C/W	
Operating Junction Temperature	TJ	+150	°C	
Operating Ambient Temperature (Note 2) MC34025 MC33025	T <sub>A</sub>	0 to +70 -40 to +105	°C	
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	_	

**ELECTRICAL CHARACTERISTICS** ( $V_{CC}$  = 15 V,  $R_T$  = 3.65 k $\Omega$ ,  $C_T$  = 1.0 nF, for typical values  $T_A$  = +25°C, for min/max values  $T_A$  is the operating ambient temperature range that applies [Note 4], unless otherwise noted.)

V <sub>IO</sub> I <sub>IB</sub> I <sub>IO</sub> A <sub>VOL</sub> GBW	- - - 60 4.0	- 0.6 0.1 95	15 3.0 1.0	mV μA μA dB
I <sub>IB</sub> I <sub>IO</sub> A <sub>VOL</sub>		0.1 95	3.0	μA μA dB
I <sub>IO</sub>		0.1 95		μA dB
A <sub>VOL</sub>		95	1.0	dB
			-	1
GBW	4.0	0.2		
	10	8.3	_	MHz
CMRR	75	95	-	dB
PSRR	85	110	-	dB
I <sub>Source</sub> I <sub>Sink</sub>	0.5 1.0	3.0 3.6	- -	mA
₩52₽.7 750 V <sub>OL</sub>	=59 <b>9</b> . <b>3</b> 27.9	.368 <b>4.53</b> 8.80 0.4	94 T <b>5</b> 0 <b>0</b> Tc(7 1.0	754 3.978 60
	PSRR I <sub>Source</sub> I <sub>Sink</sub> W520.7 75	PSRR 85  I <sub>Source</sub> 0.5 I <sub>Sink</sub> 1.0  I/520.7 75 = 598.327.9	PSRR 85 110  I <sub>Source</sub> 0.5 3.0 I <sub>Sink</sub> 1.0 3.6  I/S <sub>2</sub> 0.7 75 =59 <b>9.3</b> 27.9 368 <b>8.33</b> 8.80	PSRR 85 110 -  I <sub>Source</sub> 0.5 3.0 - I <sub>Sink</sub> 1.0 3.6 -  1/520.7 75 = 599.327.9.3688.338.8094 T50 Tc(



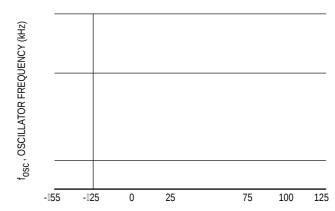
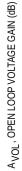
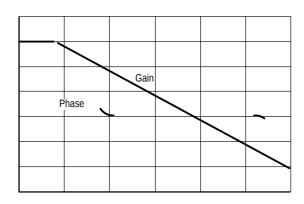
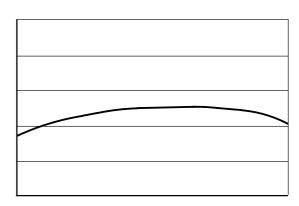
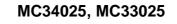


Figure 2. Timing Resistor versus Oscillator Frequency









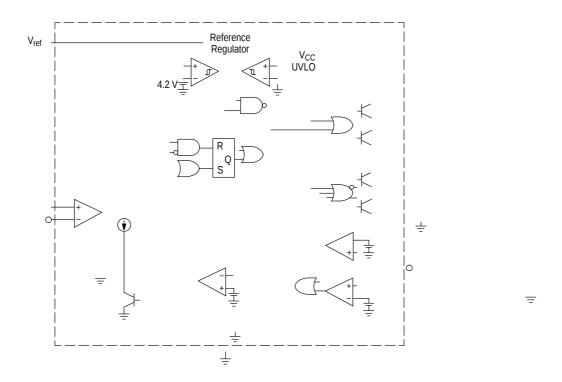
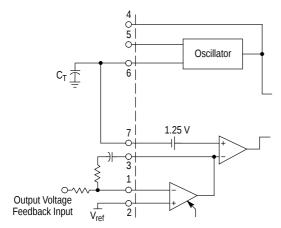


Figure 19. Representative Block Diagram

If the voltage at this pin exceeds comparator is activated. This comparat in turn, causes the Soft–	s 1.4 V, the second tor sets a latch which,	

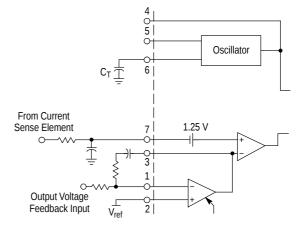
#### PIN FUNCTION DESCRIPTION

Pin No.		
DIP/SOIC	Function	Description
1	Error Amp Inverting Input	This pin is usually used for feedback from the output of the power supply.
2	Error Amp Noninverting Input	This pin is used to provide a reference in which an error signal can be produced on the output of the error amp. Usually this is connected to $V_{\text{ref}}$ , however an external reference can also be used.
3	Error Amp Output	This pin is provided for compensating the error amp for poles and zeros encountered in the power supply system, mostly the output LC filter.
4	Clock	This is a bidirectional pin used for synchronization.
5	R <sub>T</sub>	The value of R <sub>T</sub> sets the charge current through timing Capacitor, C <sub>T</sub> .
6	C <sub>T</sub>	In conjunction with $R_T$ , the timing Capacitor sets the switching frequency. Because this part is a push–pull output, each output runs at one–half the frequency set at this pin.
7	Ramp Input	For voltage mode operation this pin is connected to $C_T$ . For current mode operation this pin is connected through a filter to the current sensing element.
8	Soft-Start	A capacitor at this pin sets the Soft–Start time.
9	Current Limit/Shutdown	This pin has two functions. First, it provides cycle-by-cycle current limiting. Second, if the current is excessive, this pin will reinitiate a Soft-Start cycle.
10	Ground	This pin is the ground for the control circuitry.
11	Output A	This is a high current totem pole output.
12	Power Ground	This is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
13	V <sub>C</sub>	This is a separate power source connection for the outputs that is connected back to the power source input. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
14	Output B	This is a high current totem pole output.
15	V <sub>CC</sub>	This pin is the positive supply of the control IC.
16	V <sub>ref</sub>	This is a 5.1 V reference. It is usually connected to the noninverting input of the error amplifier.



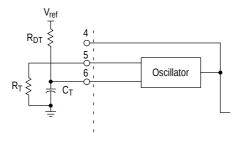
In voltage mode operation, the control range on the output of the Error Amplifier from 0% to 90% duty cycle is from 2.25 V to 4.05 V.

Figure 22. Voltage Mode Operation



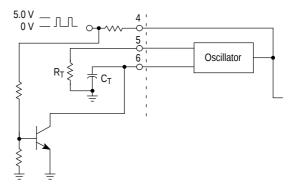
In current mode control, an RC filter should be placed at the ramp input to filter the leading edge spike caused by turn–on of a power MOSFET.

Figure 23. Current Mode Operation



Additional dead time can be added by the addition of a dead time resistor from  $V_{\text{ref}}$  to  $C_{\text{T}}$ . See text on oscillator section for more information.

Figure 24. Dead Time Addition

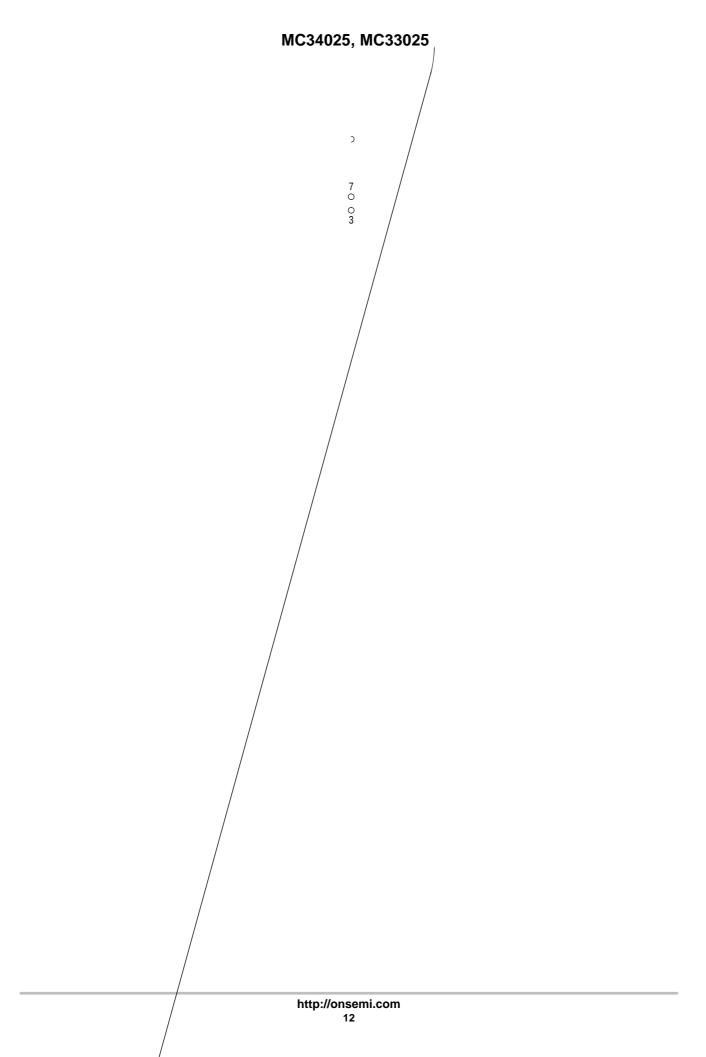


The sync pulse fed into the clock pin must be at least 3.9 V.  $R_T$  and  $C_T$  need to be set 10% slower than the sync frequency. This circuit is also used in voltage mode operation for master/slave operation. The clock signal would be coming from the master which is set at the desired operating frequency, while the slave is set 10% slower.

Figure 25. External Clock Synchronization



Figure 26. Resistive Current Sensing



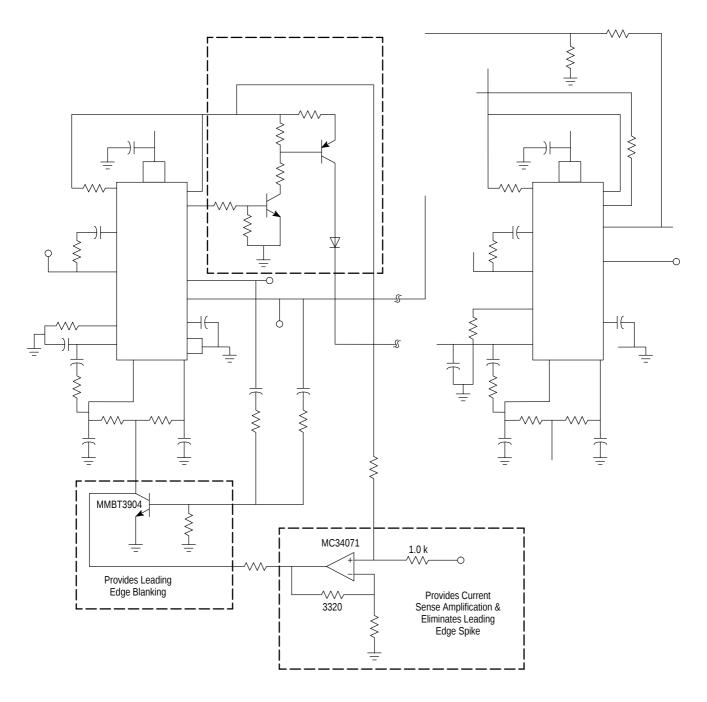
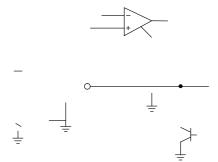
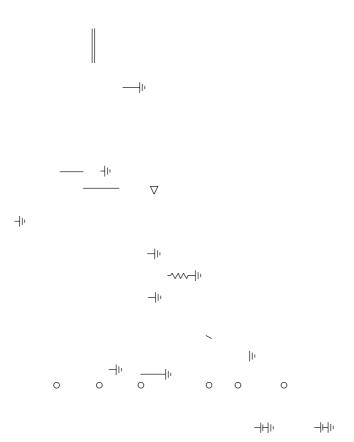
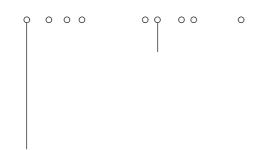


Figure 31. Synchronization Over Long Distances









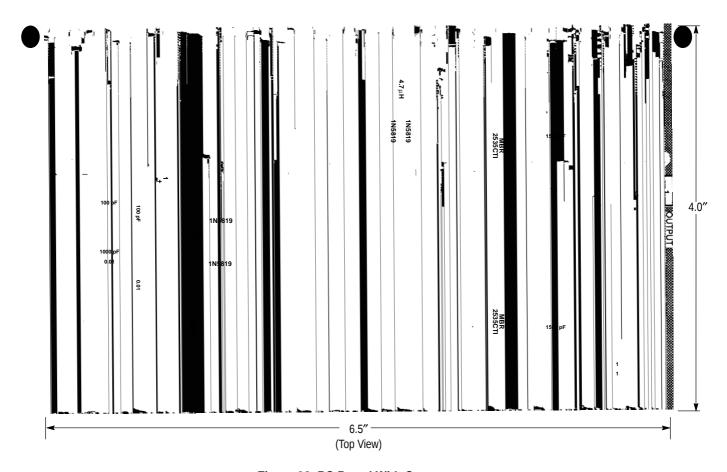
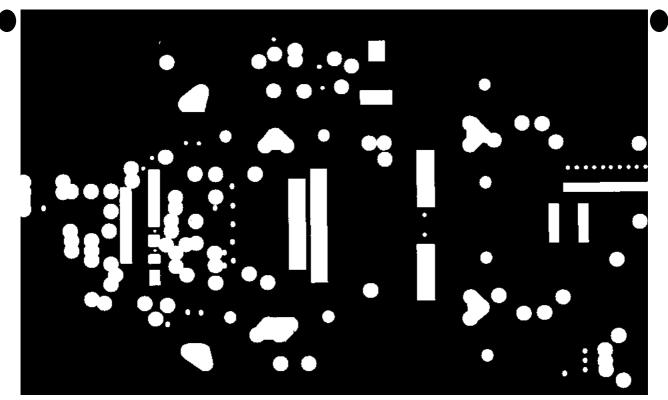


Figure 38. PC Board With Components



(Top View)

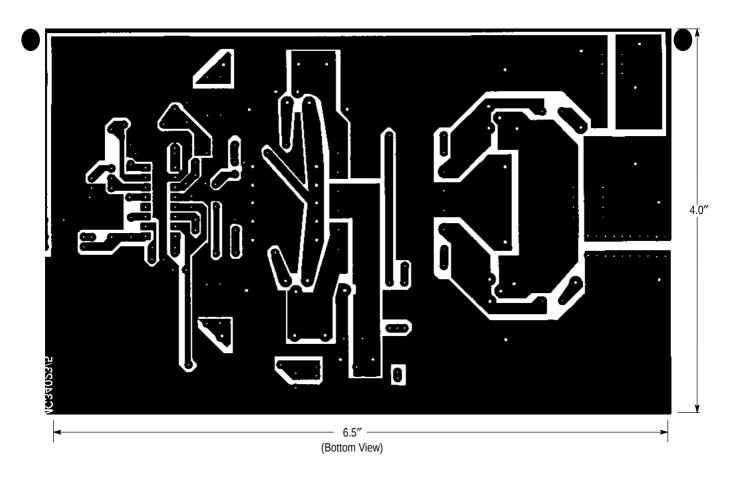


Figure 39. PC Board Without Components

#### **ORDERING INFORMATION**

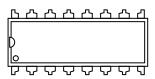
Device	Package	Shipping <sup>†</sup>
MC33025DWG	SOIC-16WB (Pb-Free)	47 Units / Rail
MC33025DWR2G	SOIC-16WB (Pb-Free)	1000 Units / Tape & Reel
MC33025PG	PDIP-16 (Pb-Free)	25 Units / Rail
MC34025DWG	SOIC-16WB (Pb-Free)	47 Units / Rail
MC34025DWR2G	SOIC-16WB (Pb-Free)	1000 Units / Tape & Reel
MC34025PG	PDIP-16 (Pb-Free)	25 Units / Rail

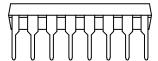
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



PDIP-16 CASE 648-08 ISSUE V

DATE 22 APR 2015





STYLE 1:

# GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code A = Assembly Location

WL = Wafer Lot
 YY = Year
 WW = Work Week
 G = Pb-Free Package

<sup>\*</sup>This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot " •", may or may not be present.



SCALE 1:1

16 9 \frac{1}{1} \tag{1} \tag{1} \tag{2} \tag{1} \tag{2} \tag{2} \tag{3} \tag{5}

#### GENERIC MARKING DIAGRAM\*

