# Critical Conduction GreenLine<sup>™</sup> SMPS<br>Controller

The MC33364 series are variable frequency SMPS controllers that operate in the critical conduction mode. They are optimized for high density power supplies requiring minimum board area, reduced component count, and low power dissipation. Integration of the high voltage startup saves approximately 0.7 W of power compared to the value of the resistor bootstrapped circuits.

Each MC33364 features an on-enthis is a Pb-Free and Halide-Free Device



**http://onsemi.com**

**MARKING**

#### **ORDERING INFORMATION**



†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### **PIN CONNECTIONS**





Figure 1. Representative Block Diagram



**Figure 3. Timing Diagram in Fault Condition**

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RESISTOR (k )

100 1000 1000

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### **MC33364**

#### **APPLICATION INFORMATION**

#### **Design Example**

Design an off--line Flyback converter according to the following requirements:

Output Power: 12 W Output: 6.0 V @ 2 Amperes Input voltage range: 90 Vac - 270 Vac, 50/60 Hz

The operation for the circuit shown in Figure 12 is as follows: the rectifier bridge D1-D4 and the capacitor C1 convert the ac line voltage to dc. This voltage supplies the primary winding of the transformer T1 and the startup circuit in U1 through the line pin. The primary current loop is closed by the transformer's primary winding, the TMOS switch Q1 and the current sense resistor R7. The resistors R5, R6, diode D6 and capacitor C4 create a snubber clamping network that protects Q1 from spikes on the primary winding. The network consisting of capacitor C3, diode D5 and resistor R1 provides a  $V_{CC}$  supply voltage for U1 from the auxiliary winding of the transformer. The resistor R1 makes  $V_{CC}$ 

The primary inductance value is given by:

$$
L_p = \frac{\max V_{in(min)}}{I_{ppk} f_{min}} = \frac{0.5127 \text{ V}}{0.472 \text{ A } 70 \text{ kHz}} = 1.92 \text{ mH}
$$

The manufacturer recommends for that magnetic core a maximum operating flux density of:<br>p

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The MOC8102 has a typical current transfer ratio (CTR) of 100% with 25% tolerance. When the TL431 is full-on, 5 mA will be drawn from the transistor within the MOC8102. The transistor should be in saturated state at that time, so its collector resistor must be

$$
R_{\text{collector}} = \frac{V_{\text{ref}} - V_{\text{sat}}}{I_{\text{LED}}} = \frac{5.0 \text{ V} - 0.3 \text{ V}}{5.0 \text{ mA}} = 940
$$

Since a resistor of 5.0 k is internally connected from the reference voltage to the feedback pin of the MC33364, the external resistor can have a higher value

$$
R_{ext} = R3 = \frac{(R_{int})(R_{collector})}{(R_{int}) - (R_{collector})} = \frac{(5.0 \text{ k})(940)}{5.0 \text{ k} - 940} = 1157 \qquad 1200
$$

This completes the design of the voltage feedback circuit.

In no load condition there is only a current flowing through the optoisolator diode and the voltage sense divider on the secondary side.

The load at that condition is given by:

$$
R_{\text{noload}} = \frac{V_{\text{out}}}{(I_{\text{LED}} + I_{\text{div}})}
$$
  
=  $\frac{6.0 \text{ V}}{(5.0 \text{ mA} + 0.25 \text{ mA})} = 1143$ 

The output filter pole at no load is:

$$
{}^{f}ph = \frac{1}{(2 \text{ R}_{\text{noload}} C_{\text{out}})}
$$
  
=  $\frac{1}{(2)(1143)(300 \text{ mF})}$  = 0.46 Hz

In heavy load condition the  $I_{LED}$  and  $I_{div}$  is negligible. The heavy load resistance is given by:

$$
R_{\text{heavy}} = \frac{V_{\text{out}}}{I_{\text{out}}} = \frac{6.0 \text{ V}}{2.0 \text{ A}} = 3.0
$$

The output filter pole at heavy load of this output is

$$
f_{\text{ph}} = \frac{1}{(2 \text{ R}_{\text{heavy}} C_{\text{out}})} = \frac{1}{(2)(3)(300 \text{ mF})} = 177 \text{ Hz}
$$

The gain exhibited by the open loop power supply at the high input voltage will be:

$$
A = \frac{V_{in max} - V_{out}}{(V_{in max})(V_{error})(Np)} = \frac{382 V - 6.0 V^{2}(7)}{(382 V)(1.2 V)(139)}
$$
  
= 15.53 = 23.82 dB

The maximum recommended bandwidth is approximately:

$$
f_C = \frac{fs \text{ min}}{5} = \frac{70 \text{ kHz}}{5} = 14 \text{ kHz}
$$

The gain needed by the error amplifier to achieve this bandwidth is calculated at the rated load because that yields the bandwidth condition, which is:

$$
Gc = 20 \log \frac{f_c}{f_{ph}} - A = 20 \log \frac{14 \text{ kHz}}{177} - 23.82 \text{ dB}
$$

$$
= 14.14 \text{ dB}
$$

The gain in absolute terms is:

$$
A_{\rm C} = 10^{\rm (G\alpha/20)} = 10^{(14.14/20)} = 5.1
$$

Now the compensation circuit elements can be calculated. The output resistance of the voltage sense divider is given by the parallel combination of resistors in the divider:

$$
R_{in} = R_{upper} \| R_{lower} = 10 k \| 14 k = 5833
$$
  
\n
$$
R9 = (Ac) (R_{in}) = 29.75 k \t 30 k
$$
  
\n
$$
C8 = \frac{1}{2 (A_C) (R_{in}) (f_C)} = 382 pF \t 390 pF
$$

The compensation zero must be placed at or below the light load filter pole:

$$
C7 = \frac{1}{2 \text{ (R9) (f}_{pn})} = 11.63 \text{ mF} \qquad 10 \text{ mF}
$$



**Figure 12. Circuit in the Design Example**







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- NOTES:<br>
1. DMENSIONING AND TOLERANCING PER ANSI<br>
2. CONTROLLING DIMENSION: MILLIMETER.<br>
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD<br>
PROTRUSION.<br>
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER<br>
SIDE.<br>
5. DIMENSION D DOES NOT IN



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