

MC1489, MC1489A

Quad Line EIA-232D Receivers

The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. EIA-232D.

Features

- Input Resistance – 3.0 k to 7.0 k Ω
- Input Signal Range –

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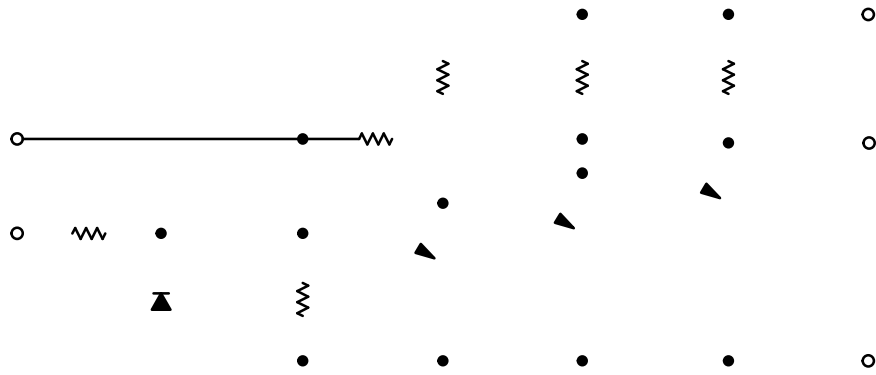


Figure 2. Representative Schematic Diagram
(1/4 of Circuit Shown)

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MAXIMUM RATINGS (T_A = + 25°C, unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	10	Vdc
Input Voltage Range	V _{IR}	± 30	Vdc

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TEST CIRCUITS

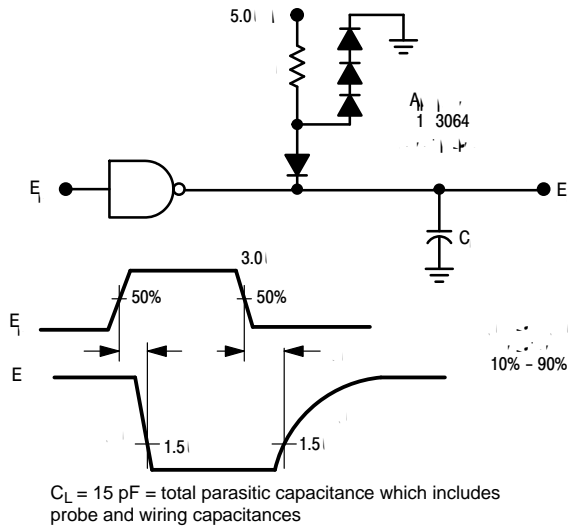


Figure 3. Switching Response

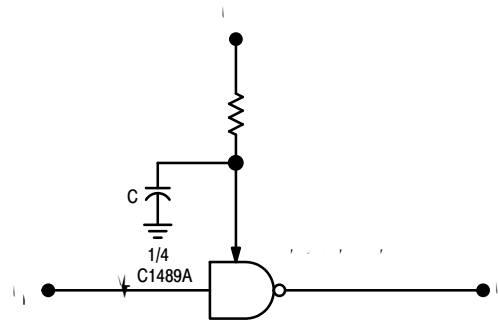


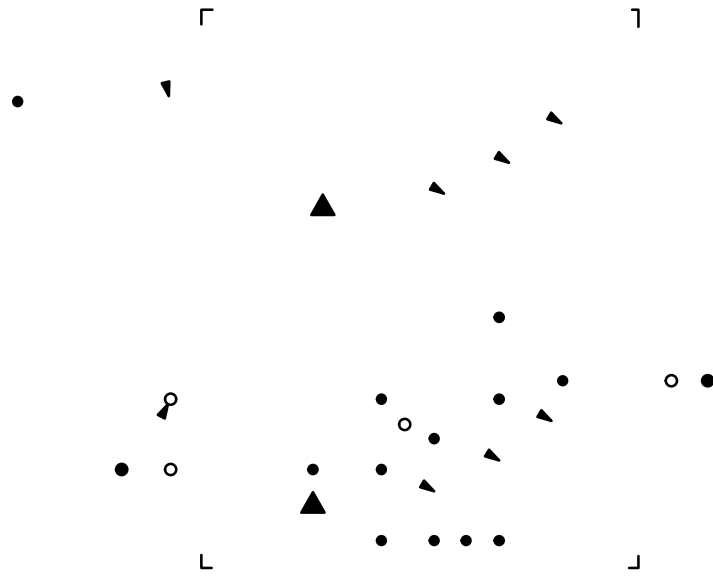
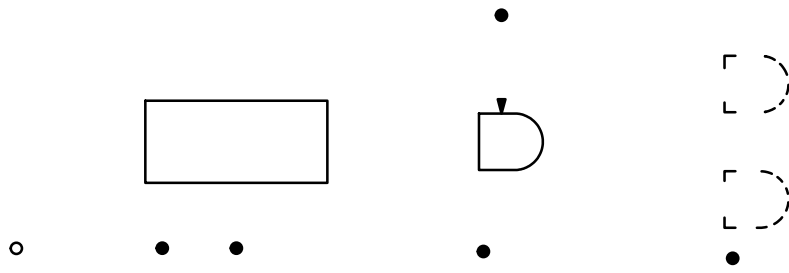
Figure 4. Response Control Node

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TYPICAL CHARACTERISTICS

($V_{CC} = 5.0 \text{ Vdc}$, $T_A = +25^\circ$)

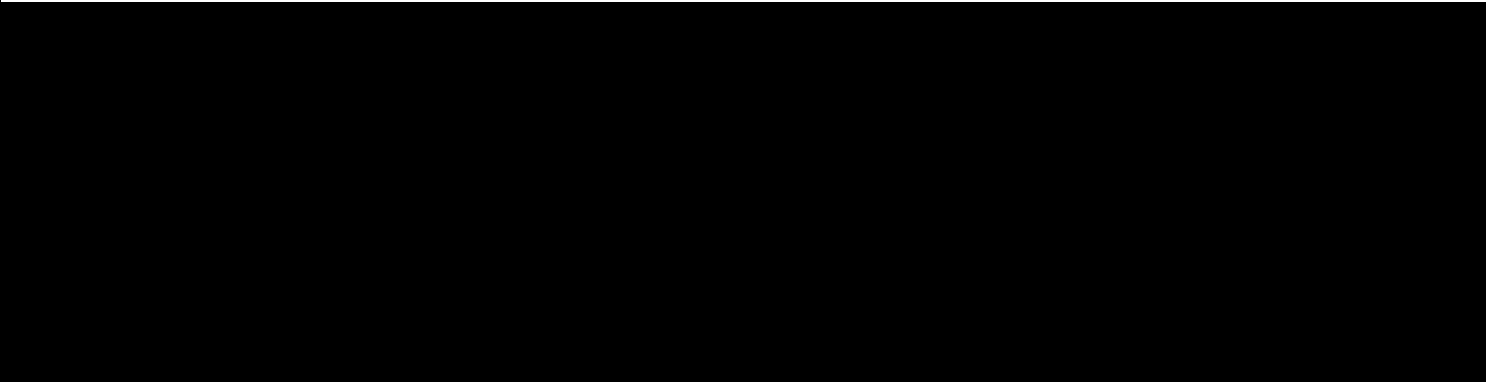
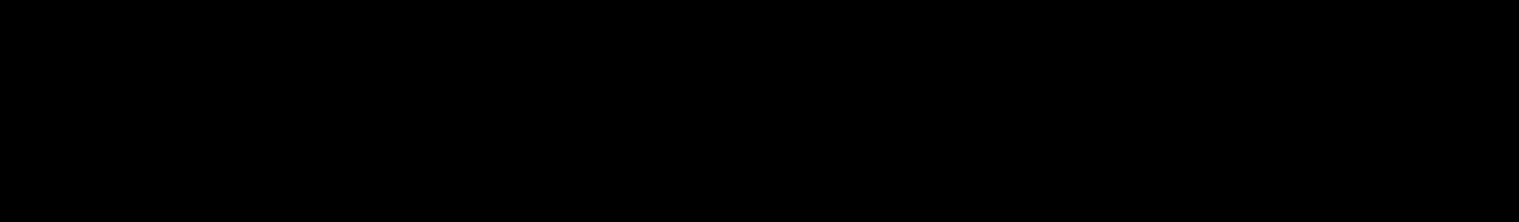
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ORDERING INFORMATION

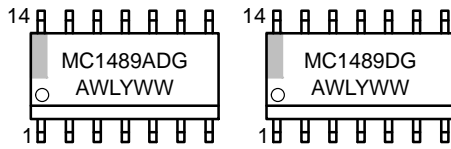
Device	Package	Operating Temperature Range	Shipping†
MC1489D	SOIC-14	$T_A = 0 \text{ to } +75^\circ\text{C}$	55 Units/Rail
MC1489DG	SOIC-14 (Pb-Free)		
MC1489DR2	SOIC-14		2500 Tape & Reel
MC1489DR2G	SOIC-14 (Pb-Free)		
MC1489AD	SOIC-14		55 Units/Rail
			2500 Tape & Reel
			25 Units/Rail
MC1489PG	PDIP-14 (Pb-Free)		
	Free		



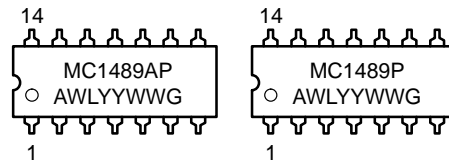
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MARKING DIAGRAMS

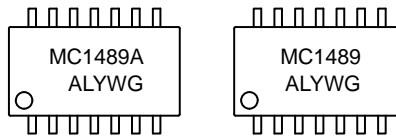
SOIC-14
D SUFFIX
CASE 751A



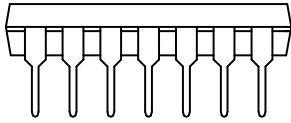
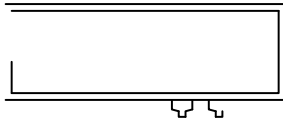
PDIP-14
P SUFFIX
CASE 646



SOEIAJ-14
M SUFFIX
CASE 965



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package



STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO
CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO
CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

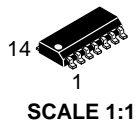
STYLE 6:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 7:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON
CATHODE

STYLE 8:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

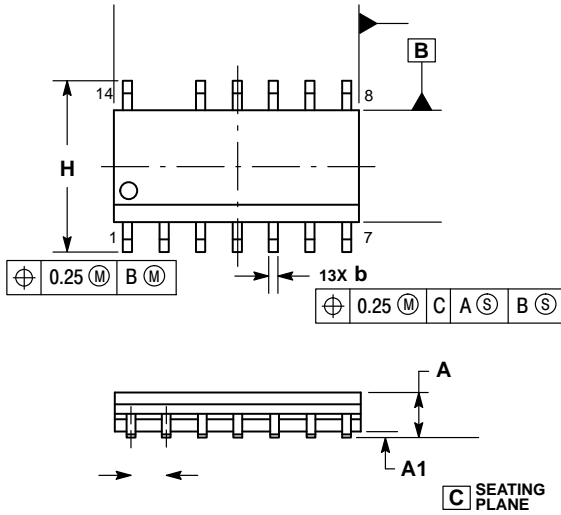
STYLE 10:
PIN 1. COMMON
CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION

9. ANODE/CATHODE



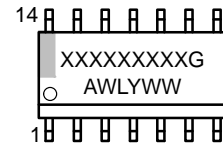
SOIC 14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

STYLES ON PAGE 2


SOIC 14
CASE 751A-03
ISSUE L

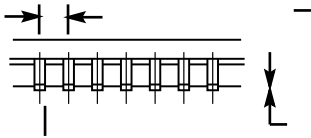
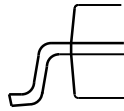
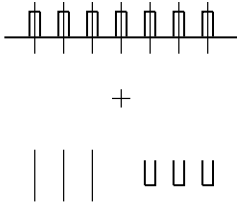
DATE 03 FEB 2016

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE

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