# **-2** 2

The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. EIA-232D.

### **Features**

- Current Limited Output ±10 mA typical
- Power–Off Source Impedance 300 Ω minimum
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range
- Compatible with All ON Semiconductor DTL and TTL Logic Families





## http://onsemi.com



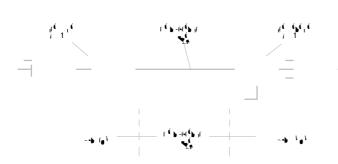
SOIC 14 D SUFFIX CASE 751A



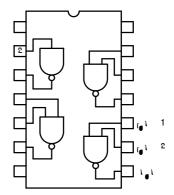
PDIP 14 P SUFFIX CASE 646



SOEIAJ 14 M SUFFIX CASE 965



### **PIN CONNECTIONS**

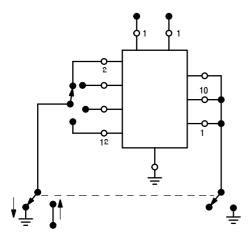


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
		₩ ₩	
		±	
۰	θ		0
			0
			0

ECTRICAL CHARACTERISTICS ±	±		0		
Characteristic	Symbol	Min	Тур	Max	Uni
					μ
$\Omega \ \Omega$					
$\Omega$					
					†
±					
∞					
∞					
					μ
					μ
					-
TITCHING CHARACTERISTICS ±	±	0			1

# **CHARACTERISTIC DEFINITIONS**



### **APPLICATIONS INFORMATION**

The Electronic Industries Association EIA–232D specification details the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the EIA–232D defined levels. The EIA–232D requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between

2. Power Supply Range – as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power supplies. In fact, the positive supply can vary from a minimum 7.0 V (required for driving the negative pulldown section) to the maximum specified 15 V. The negative supply can vary from approximately – 2.5 V to the minimum specified – 15 V. The

MC1488 will drive the output to within 2.0 V of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current limiting and supply voltage 235 Tw[driving)0 TDTf12.44280.9(the)(2.44280.9(the)(2.44280.9)

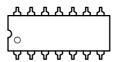
## **ORDERING INFORMATION**

Device	Package	Operating Temperature Range	Shipping
		_	
		_	
		•	
		-	
		-	
		-	

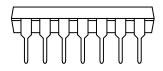
# **MARKING DIAGRAMS**

SOIC 14 D SUFFIX CASE 751A

PDIP 14 P SUFFIX CASE 646







STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO
CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO
CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR STYLE 2: STYLE 3: CANCELLED

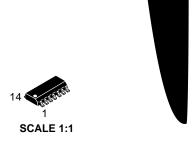
STYLE 7:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON STYLE 8:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION STYLE 6:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. NANODE/CATHODE
8. NANODE/CATHODE
8. NANODE/CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION 10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION 14. COMMON ANODE 14. COMMON CATHODE 14. COMMON ANODE

CANCELLED

STYLE 10: PIN 1. COMMON CATHODE

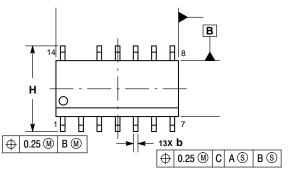
- 2. ANODE/CATHODE
  3. ANODE/CATHODE
  4. ANODE/CATHODE
  5. ANODE/CATHODE
  6. NO CONNECTION

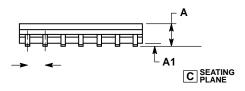
- 9. ANODE/CATHODE

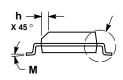


SOIC 14 NB CASE 751A-03 **ISSUE L** 

### **DATE 03 FEB 2016**







- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

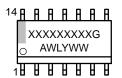
  2. CONTROLLING DIMENSION: MILLIMETERS.

  3. DIMENSION & DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.

  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.

  5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
- SIDE.

# **GENERIC MARKING DIAGRAM\***



XXXXX = Specific Device Code Α = Assembly Location

WL= Wafer Lot Υ = Year WW = Work Week G = Pb-Free Package

**STYLES ON PAGE 2** 

## SOIC 14 CASE 751A-03 ISSUE L

DATE 03 FEB 2016

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE

DOCUMENT NUMBER: 98ASH70108A

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