The MC14521B consists of a chain of 24 flip−flops with an input circuit that allows three modes of operation. The input will function as a crystal oscillator, an RC oscillator, or as an input buffer for an external oscillator. Each flip−flop divides the frequency of the previous flip−flop by two, consequently this part will count up to $2^{24} = 16{,}777{,}216$. The count advances on the negative going edge of the clock. The outputs of the last seven−stages are available for added flexibility.

Features

- All Stages are Resettable
- Reset Disables the RC Oscillator for Low Standby Power Drain
- RC and Crystal Oscillator Outputs Are Capable of Driving External Loads
- Test Mode to Reduce Test Time
- V_{DD}' and V_{SS}' Pins Brought Out on Crystal Oscillator Inverter to Allow the Connection of External Resistors for Low−Power Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load over the Rated Temperature Range
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This Device is Pb−Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	−0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V_{in}, V_{out}	−0.5 to V_{DD} +0.5	V
Input or Output Current (DC or Transient) per Pin	I_{in}, I_{out}	±10	mA
Power Dissipation, per Package (Note 1)	P_D	500	mW
Ambient Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Lead Temperature (8−Second Soldering)	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: “D/DW” Package: –7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

July, 2014 − Rev. 10
Publication Order Number:
MC14521B/D

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time (Counter Outputs)	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	–	40	80	
Propagation Delay Time	t_{PHL}, t_{PLH}					μs
Clock to Q18						
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 4415 ns		5.0	–	4.5	9.0	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 1667 ns		10	–	1.7	3.5	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 1275 ns		15	–	1.3	2.7	
Clock to Q24						
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 5915 ns		5.0	–	6.0	12	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 2167 ns		10	–	2.2	4.5	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 1675 ns		15	–	1.7	3.5	
Propagation Delay Time	t_{PHL}					ns
Reset to Q_n						
t_{PHL} = (1.7 ns/pF) C_L + 1215 ns		5.0	–	1300	2600	
t_{PHL} = (0.66 ns/pF) C_L + 467 ns		10	–	500	1000	
t_{PHL} = (0.5 ns/pF) C_L + 350 ns		15	–	375	750	
Clock Pulse Width	$t_{WH(cl)}$	5.0	385	140	–	ns
		10	150	55	–	
		15	120	40	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.5	2.0	MHz
		10	–	9.0	5.0	
		15	–	12	6.5	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	5.0	
		15	–	–	4.0	
Reset Pulse Width	$t_{WH(R)}$	5.0	1400	700	–	ns
		10	600	300	–	
		15	450	225	–	
Reset Removal Time	t_{rem}	5.0	30	–200	–	ns
		10	0	–160	–	
		15	– 40	–110	–	

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

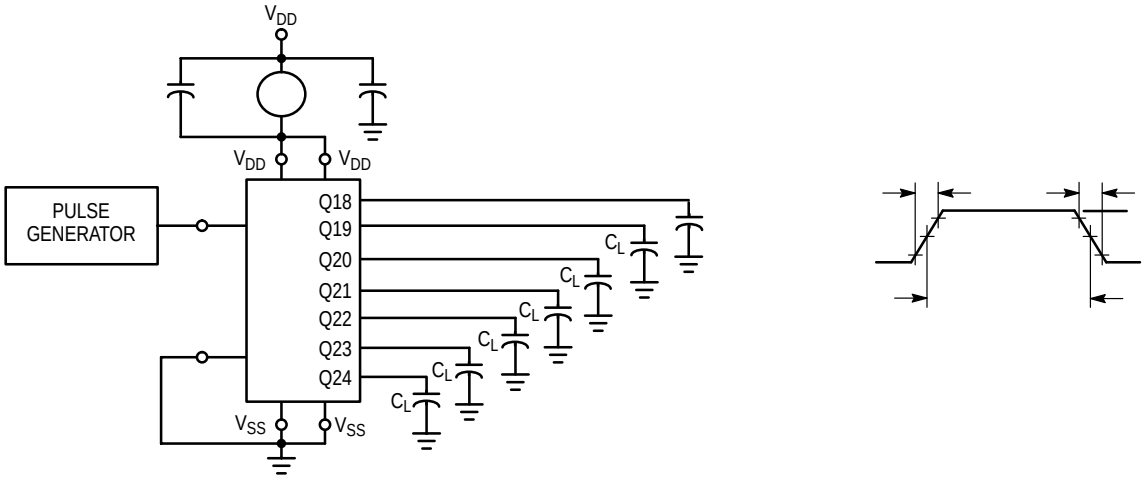


Figure 1. Power Dissipation Test Circuit and Waveform

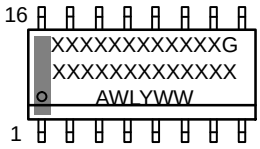
Figure 2. Switching Time Test Circuit and Waveforms

SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

S 1:
1. C C
2. BAS
3.
4. C C
5.
6. BAS
7. C C
8. C C
9. BAS
10.
11. C C
12.
13. BAS
14. C C
15.
16. C C

S 2:
1. CA
2. A
3. C C
4. CA
5. CA
6. C C
7. A
8. CA
9. CA
10. A
11. C C
12. CA
13. CA
14. C C
15. A
16. CA

S 3:
1. C C , #1
2. BAS , #1
3. , #1
4. C C , #1
5. C C , #2
6. BAS , #2
7. , #2
8. C C , #2
9. C C , #3
10. BAS , #3
11. , #3
12. C C , #3
13. C C , #4
14. BAS , #4
15. , #4
16. C C , #4

S 4:
1. C C , #1
2. C C , #1
3. C C , #2
4. C C , #2
5. C C , #3
6. C C , #3
7. C C , #4
8. C C , #4
9. BAS , #4
10. , #4
11. BAS , #3
12. , #3
13. BAS , #2
14. , #2
15. BAS , #1
16. , #1

S 5:
1. A , #1
2. A , #1
3. A , #2
4. A , #2
5. A , #3
6. A , #3
7. A , #4
8. A , #4
9. A , #4
10. S C , #4
11. A , #3
12. S C , #3
13. A , #2
14. S C , #2
15. A , #1
16. S C , #1

S 6:
1. CA
2. CA
3. CA
4. CA
5. CA
6. CA
7. CA
8. CA
9. A
10. A
11. A
12. A
13. A
14. A
15. A
16. A

S 7:
1. S C -C
2. C A ( )
3. C A ( )
4. A -C
5. C A ( )
6. C A ( )
7. C A ( )
8. S C -C
9. S C -C
10. C A ( )
11. C A ( )
12. C A ( )
13. A -C
14. C A ( )
15. C A ( )
16. S C -C

DOCUMENT NUMBER:	**98ASB42566B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOIC−16 9.90X3.90X1.50 1.27P**		**PAGE 2 OF 2**