Hex Level Shifter for TTL to CMOS or CMOS to CMOS

MC14504B

The MC14504B is a hex non inverting level shifter using CMOS technology. The level shifter will shift a TTL signal to CMOS logic levels for any CMOS supply voltage between 5 and 15 volts. A control input also allows interface from CMOS to CMOS at one logic level to another logic level: Either up or down level translating is accomplished by selection of power supply levels V_{DD} and V_{CC}. The V_{CC} level sets the input signal levels while V_{DD} selects the output voltage levels.

Features

- UP Translates from a Low to a High Voltage or DOWN Translates from a High to a Low Voltage
- Input Threshold Can Be Shifted for TTL Compatibility
- No Sequencing Required on Power Supplies or Inputs for Power Up or Power Down
- 3 to 18 Vdc Operation for V_{DD} and V_{CC}
- Diode Protected Inputs to V_{SS}
- Capable of Driving Two Low Power TTL Loads or One Low Power Schottky TTL Load Over the Rated Temperature Range
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC Q100 Qualified and PPAP Capable
- These Devices are Pb Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

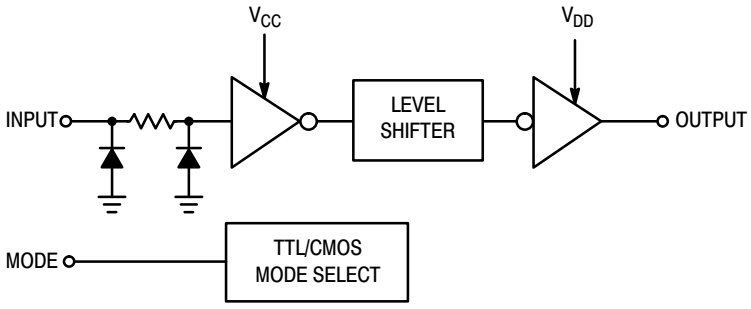
Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage Range	0.5 to +18.0	V
V_{DD}	DC Supply Voltage Range	0.5 to +18.0	V
V_{in}	Input Voltage Range (DC or Transient)	0.5 to +18.0	V
V_{out}	Output Voltage Range (DC or Transient)	0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	55 to +125	°C
T_{stg}	Storage Temperature Range	65 to +150	°C
T_L	Lead Temperature (8 Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: “D/DW” Packages: –7.0 mW/°C From 65°C To 125°C.

This device

LOGIC DIAGRAM



Mode Select	Input Logic Levels	Output Logic Levels
1 (V_{CC})	TTL	CMOS
0 (V_{SS})	CMOS	

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{CC} Vdc	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level V_{in} = 0 V	V_{OL}		5.0 10 1 5		0.05 0.05 0.05		0 0 0	0.05 0.05 0.05		0.05 0.05 0.05	Vdc
“1” Level V_{in} = V_{CC}	V_{OH}		5.0 10 15	4.95 9.95 14.95		4.95 9.95 14.95	5.0 10 15		4.95 9.95 14.95		Vdc
Input Voltage “0” Level	V_{IL}										
(V_{OL} = 1.0 Vdc) TTL CMOS		5.0	10		0.8						
(V_{OL} = 1.5 Vdc) TTL CMOS		5.0	15		0.8						
(V_{OL} = 1.0 Vdc) CMOS CMOS		5.0	10		1.5						
(V_{OL} = 1.5 Vdc) CMOS CMOS		5.0	15		1.5						
(V_{OL} = 1.5 Vdc) CMOS CMOS		10	15		3.0						

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	Shifting Mode	V_{CC} Vdc	V_{DD} Vdc	Limits			Unit
					Min	Typ (Note 3)	Max	
Propagation Delay, High to Low	t_{PHL}	TTL – CMOS $V_{DD} > V_{CC}$	5.0 5.0	10 15		140 140	280 280	ns
		CMOS – CMOS $V_{DD} > V_{CC}$	5.0 5.0 10	10 15 15		120 120 70	240 240 140	
		CMOS – CMOS $V_{CC} > V_{DD}$	10 15 15	5.0 5.0 10		185 185 175	370 370 350	
Propagation Delay, Low to High	t_{PLH}	TTL – CMOS $V_{DD} > V_{CC}$	5.0 5.0	10 15		170 160	340 320	ns
		CMOS – CMOS $V_{DD} > V_{CC}$	5.0 5.0 10	10 15 15		170 170 100	340 340 200	
		CMOS – CMOS $V_{CC} > V_{DD}$	10 15 15	5.0 5.0 10		275 275 145	550 550 290	

SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

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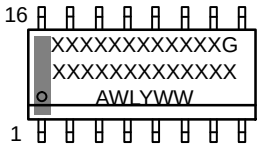
ISSUE L

DATE 29 MAY 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

S 1:
1. C C
2. BAS
3.
4. C C
5.
6. BAS
7. C C
8. C C
9. BAS
10.
11. C C
12.
13. BAS
14. C C
15.
16. C C

S 2:
1. CA
2. A
3. C C
4. CA
5. CA
6. C C
7. A
8. CA
9. CA
10. A
11. C C
12. CA
13. CA
14. C C
15. A
16. CA

S 3:
1. C C , #1
2. BAS , #1
3. , #1
4. C C , #1
5. C C , #2
6. BAS , #2
7. , #2
8. C C , #2
9. C C , #3
10. BAS , #3
11. , #3
12. C C , #3
13. C C , #4
14. BAS , #4
15. , #4
16. C C , #4

S 4:
1. C C , #1
2. C C , #1
3. C C , #2
4. C C , #2
5. C C , #3
6. C C , #3
7. C C , #4
8. C C , #4
9. BAS , #4
10. , #4
11. BAS , #3
12. , #3
13. BAS , #2
14. , #2
15. BAS , #1
16. , #1

S 5:
1. A , #1
2. A , #1
3. A , #2
4. A , #2
5. A , #3
6. A , #3
7. A , #4
8. A , #4
9. A , #4
10. S C , #4
11. A , #3
12. S C , #3
13. A , #2
14. S C , #2
15. A , #1
16. S C , #1

S 6:
1. CA
2. CA
3. CA
4. CA
5. CA
6. CA
7. CA
8. CA
9. A
10. A
11. A
12. A
13. A
14. A
15. A
16. A

S 7:
1. S C -C
2. C A ( )
3. C A ( )
4. A -C
5. C A ( )
6. C A ( )
7. C A ( )
8. S C -C
9. S C -C
10. C A ( )
11. C A ( )
12. C A ( )
13. A -C
14. C A ( )
15. C A ( )
16. S C -C

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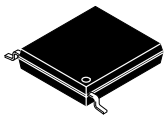

SCALE 2:1

TSSOP−16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006