March, 2022 – Rev. 12

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TRUTH TABLE

Clock	Reset	Output State
	0	No Change
~	0	Advance to next state
Х	1	All Outputs are low

X = Don't Care

LOGIC DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping [†]
MC14040BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14040BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
NLV14040BDR2G*	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
MC14040BDTR2G	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel
NLV14040BDTR2G*	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. *NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP

Capable.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}, T_A = 25^{\circ}C$)

Characteristic	Symbol	V _{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Pice and Fall Time	••••••			()		-
True True = $(1.5 \text{ ns/nE}) \text{ Cu} + 25 \text{ ns}$	ιτLH, t r uu	5.0	_	100	200	115
$T_{T_{1}\mu_{1}}$, $T_{T_{1}\mu_{1}} = (0.75 \text{ ns/pF}) C_{1} + 12.5 \text{ ns}$	THL	10	_	50	100	
$T_{T_1 H}, T_{T_1 H} = (0.55 \text{ ns/pF}) C_1 + 9.5 \text{ ns}$		15	-	40	80	
Propagation Delay Time	t _{PI H} ,					
Clock to Q1	t _{PHL}					ns
t _{PHL} , t _{PLH} = (1.7 ns/pF) C _L + 315 ns		5.0	-	260	520	
t _{PHL} , t _{PLH} = (0.66 ns/pF) C _L + 137 ns		10	-	115	230	
t _{PHL} , t _{PLH} = (0.5 ns/pF) C _L + 95 ns		15	-	80	160	
Clock to Q12						ns
t _{PHL} , t _{PLH} = (1.7 ns/pF) C _L + 2415 ns		5.0	-	1625	3250	
t _{PHL} , t _{PLH} = (0.66 ns/pF) C _L + 867 ns		10	-	720	1440	
t _{PHL} , t _{PLH} = (0.5 ns/pF) C _L + 475 ns		15	-	500	1000	
Propagation Delay Time	t _{PHL}					ns
Reset to Q _n						
t _{PHL} = (1.7 ns/pF) C _L + 485 ns		5.0	-	370	740	
$t_{PHL} = (0.86 \text{ ns/pF}) C_L + 182 \text{ ns}$		10	-	155	310	
t _{PHL} = (0.5 ns/pF) C _L + 145 ns		15	-	115	230	
Clock Pulse Width	t _{WH}	5.0	385	140	-	ns
		10	150	55	-	
		15	115	38	-	
Clock Pulse Frequency	f _{cl}	5.0	-	2.1	1.5	MHz
		10	-	7.0	3.5	
		15	-	10.0	4.5	

Clock Rise and Fall Time

t_{1.5}



Figure 3. Timing Diagram

SOIC-16 9.90x3.90x1.50 1.27P CASE 751B ISSUE L

SOIC-16 9.90x3.90x1.50 1.27P CASE 751B ISSUE L

GENERIC MARKING DIAGRAM*

16	H	- A	H.	H.	H	H.	H.	Æ
		XX)	XX)	XX)	KX)	XX)	XX	G
		XX	XX	XX	XX	XX	XX)	хI
	0		A	WĽ	YΝ	/W		
1	Ш	н	н	Н	н	П	н	╥╹

XXXXX = Specific Device Code

A = Assembly Location

- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

S	1:		S 2:			S	3:		S	4:	
	1.	C C	1.	CA			1.	C C , #1		1.	C C , #1
	2.	BAS	2.	Α			2.	BAS ,#1		2.	C C ,#1
	3.		3.	С	С		3.	,#1		3.	C C ,#2
	4.	СС	4.	CA			4.	C C ,#1		4.	C C ,#2
	5.		5.	CA			5.	C C .#2		5.	C C .#3
	6.	BAS	6.	С	С		6.	BAS .#2		6.	C C .#3
	7.	C C	7.	Α			7.	. #2		7.	C C .#4
	8.	C C	8.	CA			8.	C C .#2		8.	C C .#4
	9.	BAS	9.	CA			9.	C C ,#3		9.	BAS ,#4
	10.		10.	Α			10.	BAS , #3		10.	,#4
	11.	СС	11.	С	С		11.	, #3		11.	BAS , #3
	12.		12.	CA			12.	C C ,#3		12.	, #3
	13.	BAS	13.	CA			13.	C C ,#4		13.	BAS ,#2
	14.	C C	14.	С	C		14.	BAS ,#4		14.	, #2
	15.		15.	Α			15.	, #4		15.	BAS ,#1
	16.	C C	16.	CA			16.	C C ,#4		16.	,#1
c	<u>ج</u>		S 6.			c	7.				
J,	J. 1	Δ #1	J U.	CA		J,	1.	0.02			
	2	Δ #1	ı. 2	CA			2)		
	3	Δ #2	2.	CA			3		1		
	4	Δ #2	4	CA			4	A -C	. /		
	5	A #3	5	CA			5	C A ()		
	6	A #3	6	CA			6	C A (1		
	7	A #4	7	CA			7	C A (1		
	8	A #4	8	CA			8	S C -C	. /		
	9	A #4	9	A			9	S C -C			
	10	S C #4	10	A			10	C A ()		
	11	A #3	11	A			11	C A (1		
	12	S C #3	12	A			12	Č A	1		
	13.	A .#2	13.	A			13.	A -C	. /		
			14	٨			14	C A ()		
	14.	S (L.#2	14.	~			14.				
	14. 15.	S C,#2 A.#1	14.	Â			14.	C A (1		
	14. 15. 16.	S C,#2 A,#1 S C,#1	14. 15. 16.	A A			14. 15. 16.	C Â() S C -C	()		

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SCALE 2:1

TSSOP-16 WB CASE 948F ISSUE B

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