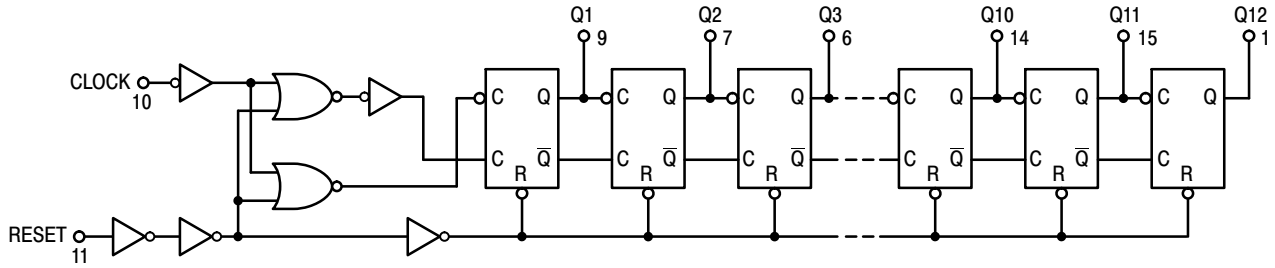
TRUTH TABLE

Clock	Reset	Output State
⎍	0	No Change
⎎	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

LOGIC DIAGRAM



Q4 = PIN 5
Q5 = PIN 3
Q6 = PIN 2
Q7 = PIN 4
Q8 = PIN 13
Q9 = PIN 12
V_{DD} = PIN 16
V_{SS} = PIN 8

ORDERING INFORMATION

Device	Package	Shipping†
MC14040BDG	SOIC−16 (Pb−Free)	48 Units / Rail
MC14040BDR2G	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel
NLV14040BDR2G*	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel
MC14040BDTR2G	TSSOP−16 (Pb−Free)	2500 Units / Tape & Reel
NLV14040BDTR2G*	TSSOP−16 (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
T_{TLH}, T_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
T_{TLH}, T_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
T_{TLH}, T_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					
Clock to Q1	t_{PHL}					ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 315 ns		5.0	–	260	520	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 137 ns		10	–	115	230	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 95 ns		15	–	80	160	
Clock to Q12						ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 2415 ns		5.0	–	1625	3250	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 867 ns		10	–	720	1440	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 475 ns		15	–	500	1000	
Propagation Delay Time	t_{PHL}					ns
Reset to Q_n						
t_{PHL} = (1.7 ns/pF) C_L + 485 ns		5.0	–	370	740	
t_{PHL} = (0.86 ns/pF) C_L + 182 ns		10	–	155	310	
t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	–	115	230	
Clock Pulse Width	t_{WH}	5.0	385	140	–	ns
		10	150	55	–	
		15	115	38	–	
Clock Pulse Frequency	f_{cl}	5.0	–	2.1	1.5	MHz
		10	–	7.0	3.5	
		15	–	10.0	4.5	
Clock Rise and Fall Time	$t_{1.5}$					

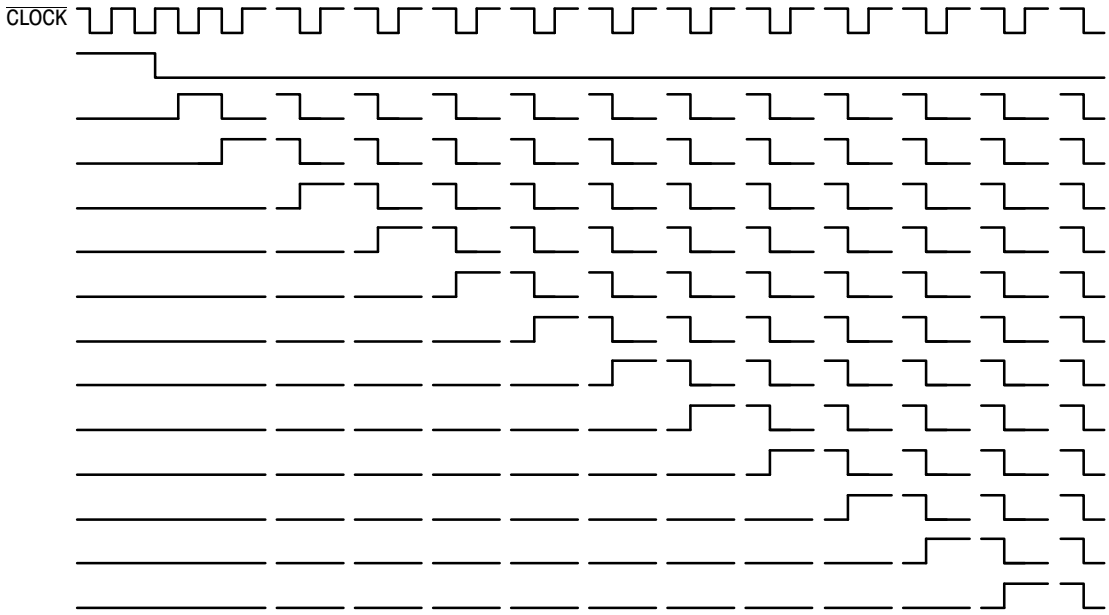


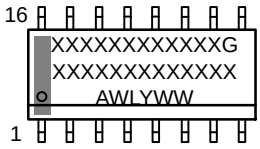
Figure 3. Timing Diagram

SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

S 1:
1. C C
2. BAS
3.
4. C C
5.
6. BAS
7. C C
8. C C
9. BAS
10.
11. C C
12.
13. BAS
14. C C
15.
16. C C

S 2:
1. CA
2. A
3. C C
4. CA
5. CA
6. C C
7. A
8. CA
9. CA
10. A
11. C C
12. CA
13. CA
14. C C
15. A
16. CA

S 3:
1. C C , #1
2. BAS , #1
3. , #1
4. C C , #1
5. C C , #2
6. BAS , #2
7. , #2
8. C C , #2
9. C C , #3
10. BAS , #3
11. , #3
12. C C , #3
13. C C , #4
14. BAS , #4
15. , #4
16. C C , #4

S 4:
1. C C , #1
2. C C , #1
3. C C , #2
4. C C , #2
5. C C , #3
6. C C , #3
7. C C , #4
8. C C , #4
9. BAS , #4
10. , #4
11. BAS , #3
12. , #3
13. BAS , #2
14. , #2
15. BAS , #1
16. , #1

S 5:
1. A , #1
2. A , #1
3. A , #2
4. A , #2
5. A , #3
6. A , #3
7. A , #4
8. A , #4
9. A , #4
10. S C , #4
11. A , #3
12. S C , #3
13. A , #2
14. S C , #2
15. A , #1
16. S C , #1

S 6:
1. CA
2. CA
3. CA
4. CA
5. CA
6. CA
7. CA
8. CA
9. A
10. A
11. A
12. A
13. A
14. A
15. A
16. A

S 7:
1. S C -C
2. C A ( )
3. C A ( )
4. A -C
5. C A ( )
6. C A ( )
7. C A ( )
8. S C -C
9. S C -C
10. C A ( )
11. C A ( )
12. C A ( )
13. A -C
14. C A ( )
15. C A ( )
16. S C -C

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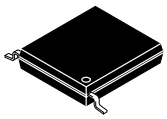
DESCRIPTION:	**SOIC−16 9.90X3.90X1.50 1.27P**		**PAGE 2 OF 2**



SCALE 2:1

TSSOP−16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006