

MC14018B

Presettable Divide-By-N Counter

The MC14018B contains five Johnson counter stages which are asynchronously presettable and resettable. The counters are synchronous, and increment on the positive going edge of the clock.

Presetting is accomplished by a logic 1 on the preset enable input. Data on the Jam inputs will then be transferred to their respective \bar{Q} outputs (inverted). A logic 1 on the reset input will cause all \bar{Q} outputs to go to a logic 1 state.

Division by any number from 2 to 10 can be accomplished by connecting appropriate \bar{Q} outputs to the data input, as shown in the Function Selection table. Anti-lock gating is included in the MC14018B to assure proper counting sequence.

Features

- Fully Static Operation
- Schmitt Trigger on Clock Input
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4018B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	-55 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



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SOIC-16
D SUFFIX
CASE 751B

MARKING DIAGRAM

14018BG
AWLYWW

- 1
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Indicator

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage $V_{in} = V_{DD}$ or 0 $V_{in} = 0$ or V_{DD}	"0" Level V_{OL}	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
		10	-	0.05	-	0	0.05	-	0.05	
		15	-	0.05	-	0	0.05	-	0.05	
	"1" Level V_{OH}	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
		10	9.95	-	9.95	10	-	9.95	-	
		15	14.95	-	14.95	15	-	14.95	-	
Input Voltage $(V_O = 4.5$ or 0.5 Vdc) $(V_O = 9.0$ or 1.0 Vdc) $(V_O = 13.5$ or 1.5 Vdc) $(V_O = 0.5$ or 4.5 Vdc) $(V_O = 1.0$ or 9.0 Vdc) $(V_O = 1.5$ or 13.5 Vdc)	"0" Level V_{IL}	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc
		10	-	3.0	-	4.50	3.0	-	3.0	
		15	-	4.0	-	6.75	4.0	-	4.0	
	"1" Level V_{IH}	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
		10	7.0	-	7.0	5.50	-	7.0	-	
		15	11	-	11	8.25	-	11	-	
Output Drive Current $(V_{OH} = 2.5$ Vdc) $(V_{OH} = 4.6$ Vdc) $(V_{OH} = 9.5$ Vdc) $(V_{OH} = 13.5$ Vdc) $(V_{OL} = 0.4$ Vdc) $(V_{OL} = 0.5$ Vdc) $(V_{OL} = 1.5$ Vdc)	Source I_{OH}	5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	mAdc
		5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	
		10	-1.6	-	-1.3	-2.25	-	-0.9	-	
		15	-4.2	-	-3.4	-8.8	-	-2.4	-	
	Sink I_{OL}	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc
		10	1.6	-	1.3	2.25	-	0.9	-	
15		4.2	-	3.4	8.8	-	2.4	-		
Input Current	I_{in}	15	-	0.1 Tm(-)TjET2698531.72(efBT8 0 0 8 284.1449 f303.761 475.994 34.6e565T2e1						

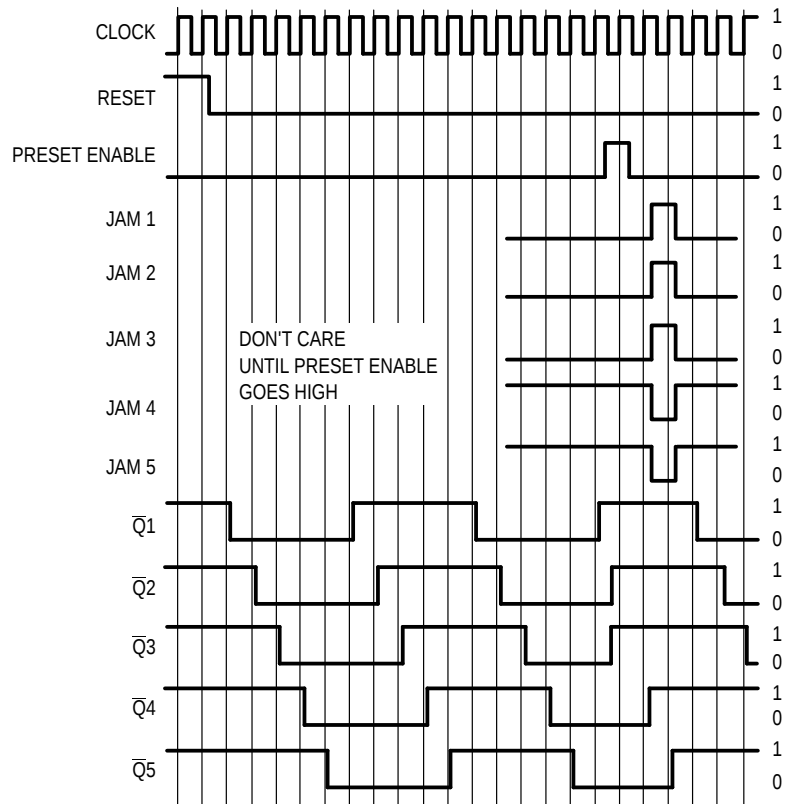
MC14018B

SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} Vdc	All Types		Unit
			Min	Typ	

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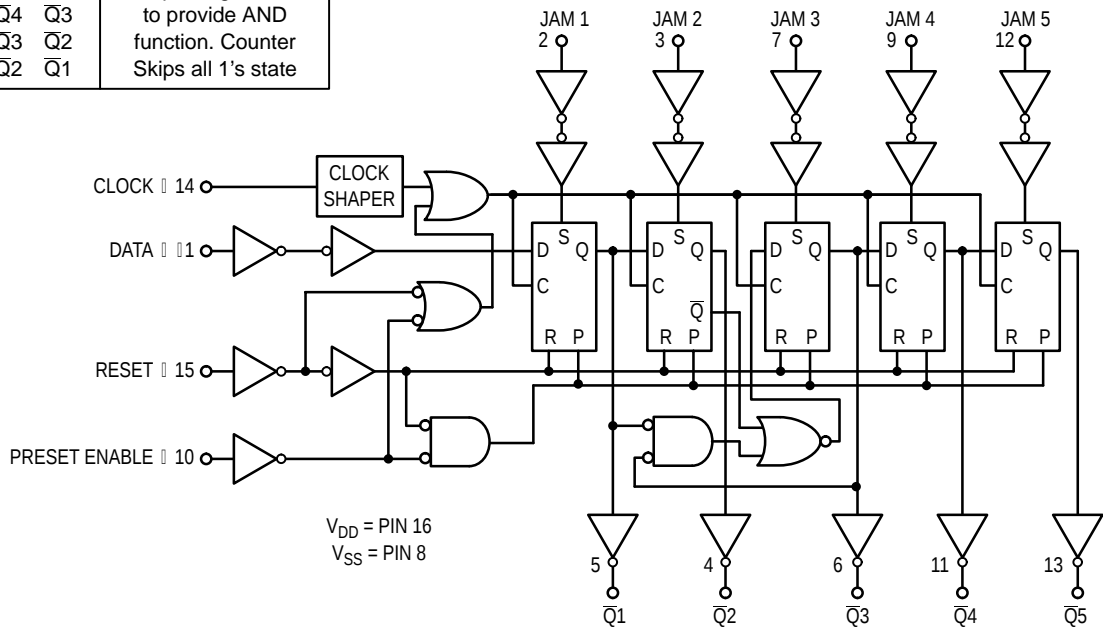
TIMING DIAGRAM
($\bar{Q}5$ Connected to Data Input)



FUNCTION SELECTION

Counter Mode	Connect Data Input (Pin 1) to:	Comments
Divide by 10 Divide by 8 Divide by 6 Divide by 4 Divide by 2	$\bar{Q}5$ $\bar{Q}4$ $\bar{Q}3$ $\bar{Q}2$ $\bar{Q}1$	No external components needed.
Divide by 9 Divide by 7 Divide by 5 Divide by 3	$\bar{Q}5$ $\bar{Q}4$ $\bar{Q}4$ $\bar{Q}3$ $\bar{Q}3$ $\bar{Q}2$ $\bar{Q}2$ $\bar{Q}1$	Gate package needed to provide AND function. Counter Skips all 1's state

LOGIC DIAGRAM

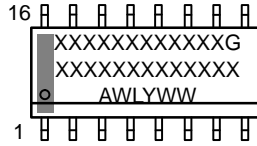


SOIC-16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

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DATE 29 MAY 2024

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

<p>S 1: 1. C C ✓ 2. BAS ✓ 3. ✓ 4. C C ✓ 5. ✓ 6. BAS ✓ 7. C C ✓ 8. C C ✓ 9. BAS ✓ 10. ✓ 11. C C ✓ 12. ✓ 13. BAS ✓ 14. C C ✓ 15. ✓ 16. C C ✓</p>	<p>S 2: 1. CA ✓ 2. A ✓ 3. C C ✓ 4. CA ✓ 5. CA ✓ 6. C C ✓ 7. A ✓ 8. CA ✓ 9. CA ✓ 10. A ✓ 11. C C ✓ 12. CA ✓ 13. CA ✓ 14. C C ✓ 15. A ✓ 16. CA ✓</p>	<p>S 3: 1. C C , #1 ✓ 2. BAS , #1 ✓ 3. , #1 ✓ 4. C C , #1 ✓ 5. C C , #2 ✓ 6. BAS , #2 ✓ 7. , #2 ✓ 8. C C , #2 ✓ 9. C C , #3 ✓ 10. BAS , #3 ✓ 11. , #3 ✓ 12. C C , #3 ✓ 13. C C , #4 ✓ 14. BAS , #4 ✓ 15. , #4 ✓ 16. C C , #4 ✓</p>	<p>S 4: 1. C C , #1 ✓ 2. C C , #1 ✓ 3. C C , #2 ✓ 4. C C , #2 ✓ 5. C C , #3 ✓ 6. C C , #3 ✓ 7. C C , #4 ✓ 8. C C , #4 ✓ 9. BAS , #4 ✓ 10. , #4 ✓ 11. BAS , #3 ✓ 12. , #3 ✓ 13. BAS , #2 ✓ 14. , #2 ✓ 15. BAS , #1 ✓ 16. , #1 ✓</p>
<p>S 5: 1. A , #1 ✓ 2. A , #1 ✓ 3. A , #2 ✓ 4. A , #2 ✓ 5. A , #3 ✓ 6. A , #3 ✓ 7. A , #4 ✓ 8. A , #4 ✓ 9. A , #4 ✓ 10. S C , #4 ✓ 11. A , #3 ✓ 12. S C , #3 ✓ 13. A , #2 ✓ 14. S C , #2 ✓ 15. A , #1 ✓ 16. S C , #1 ✓</p>	<p>S 6: 1. CA ✓ 2. CA ✓ 3. CA ✓ 4. CA ✓ 5. CA ✓ 6. CA ✓ 7. CA ✓ 8. CA ✓ 9. A ✓ 10. A ✓ 11. A ✓ 12. A ✓ 13. A ✓ 14. A ✓ 15. A ✓ 16. A ✓</p>	<p>S 7: 1. S C -C ✓ 2. C A () ✓ 3. C A () ✓ 4. A -C ✓ 5. C A () ✓ 6. C A () ✓ 7. C A () ✓ 8. S C -C ✓ 9. S C -C ✓ 10. C A () ✓ 11. C A () ✓ 12. C A () ✓ 13. A -C ✓ 14. C A () ✓ 15. C A () ✓ 16. S C -C ✓</p>	

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