

# MC14008B

## 4-B F Adder

The MC14008B 4-bit full adder is constructed with MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. This device consists of four full adders with fast internal look-ahead carry output. It is useful in binary addition and other arithmetic applications. The fast parallel carry output bit allows high-speed operation when used with other adders in a system.

### Features

- Look-Ahead Carry Output
- Diode Protection on All Inputs
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4008B
- This Device is Pb-Free and is RoHS Compliant

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 1)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating: "D/DW" Package: -7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

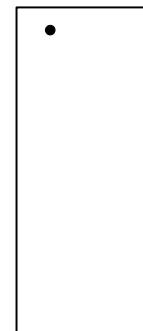
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



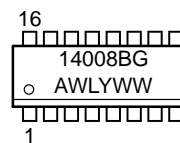
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SOIC-16  
D SUFFIX  
CASE 751B



### MARKING DIAGRAM



- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G = Pb-Free Indicator

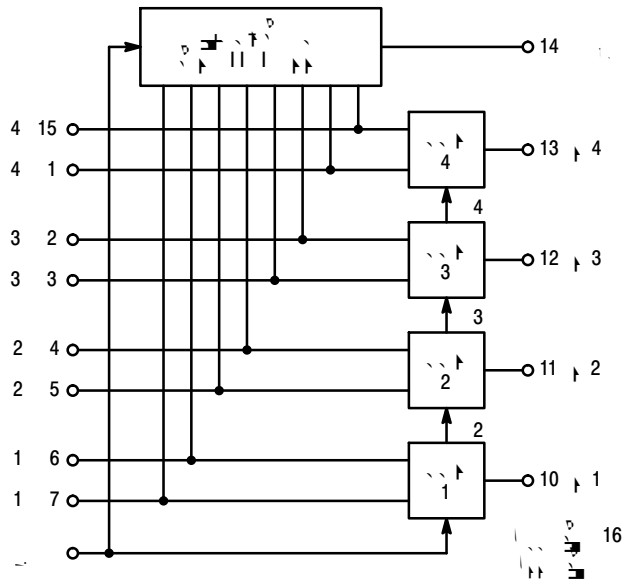
### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# MC14008B

## TRUTH TABLE

### BLOCK DIAGRAM



# MC14008B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	“0” Level V <sub>OL</sub>	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
15		–	0.05	–	0	0.05	–	0.05		
V <sub>in</sub> = 0 or V <sub>DD</sub>	“1” Level V <sub>OH</sub>	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	“0” Level V <sub>IL</sub>	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
		10	–	3.0	–	4.50	3.0	–	3.0	
		15	–	4.0	–	6.75	4.0	–	4.0	
(V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	“1” Level V <sub>IH</sub>	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
		10	7.0	–	7.0	5.50	–	7.0	–	
		15	11	–	11	8.25	–	11	–	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source I <sub>OH</sub>	5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	
		10	–1.6	–	–1.3	–2.25	–	–0.9	–	
		15	–4.2	–	–3.4	–8.8	–	–2.4	–	
	Sink I <sub>OL</sub>	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
		10	1.6	–	1.3	2.25	–	0.9	–	
15		4.2	–	3.4	8.8	–	2.4	–		
Input Current	I <sub>in</sub>	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (1.7 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (3.4 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (5.0 μA/kHz) f + I <sub>DD</sub>							μAdc
	10									
	15									

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> – V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.005.



# MC14008B

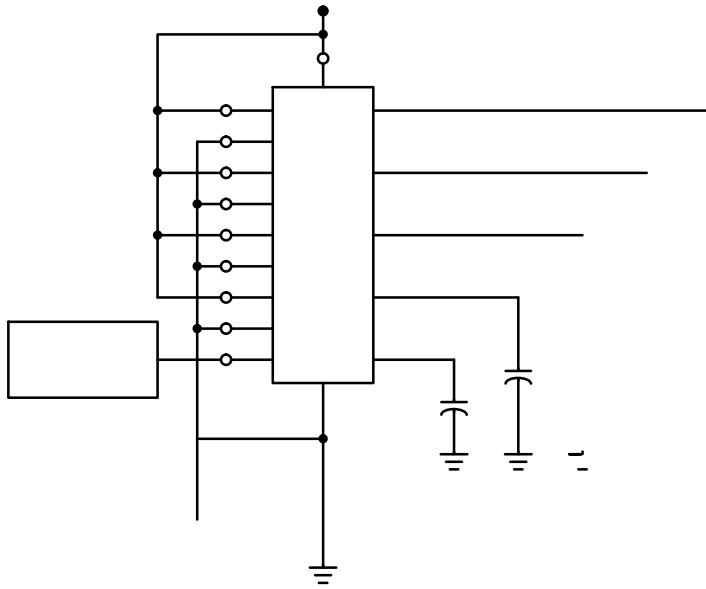


Figure 3. Dynamic Power Dissipation Test Circuit and Waveform

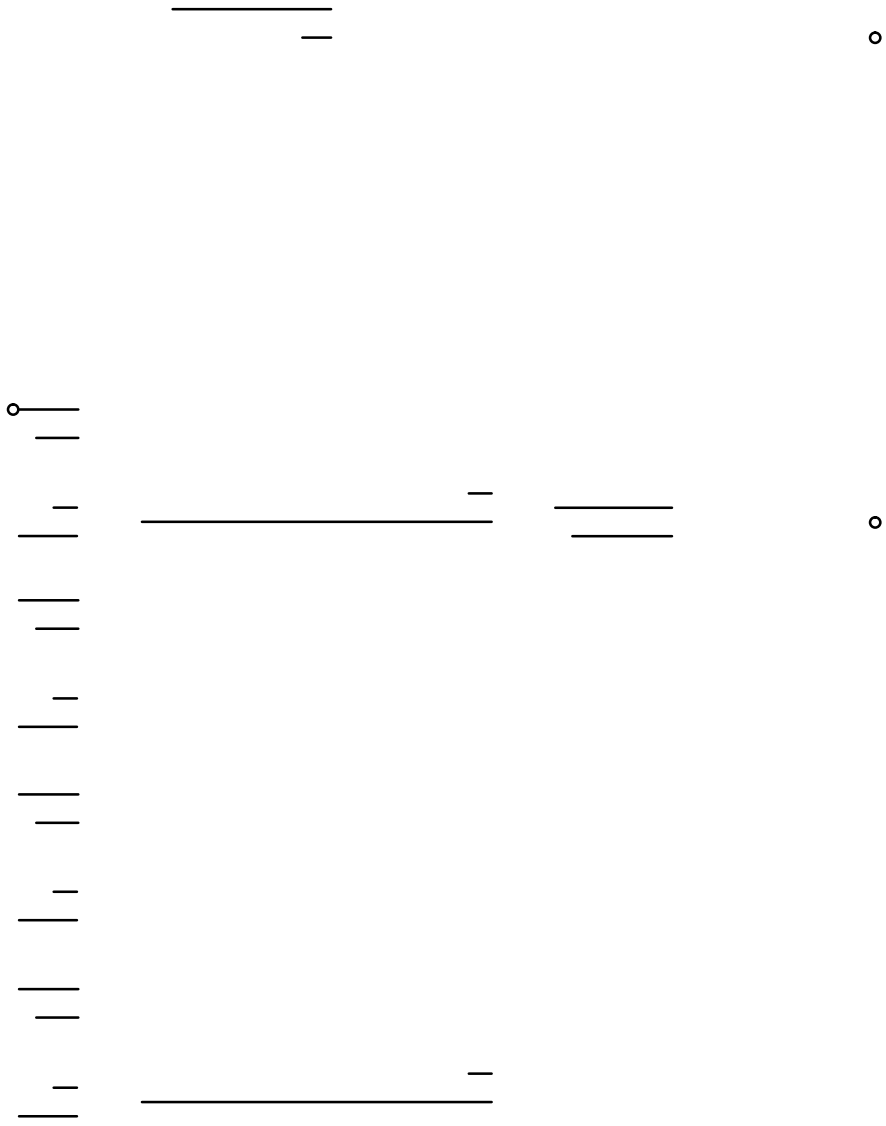


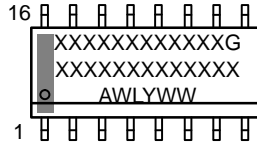
Figure 5. Logic Diagram

**SOIC-16 9.90x3.90x1.50 1.27P**  
CASE 751B  
ISSUE L

SOIC-16 9.90x3.90x1.50 1.27P  
CASE 751B  
ISSUE L

DATE 29 MAY 2024

GENERIC  
MARKING DIAGRAM\*



XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

<p>S 1: 1. C C ✓  2. BAS ✓  3. ✓  4. C C ✓  5. ✓  6. BAS ✓  7. C C ✓  8. C C ✓  9. BAS ✓  10. ✓  11. C C ✓  12. ✓  13. BAS ✓  14. C C ✓  15. ✓  16. C C ✓</p>	<p>S 2: 1. CA ✓  2. A ✓  3. C C ✓  4. CA ✓  5. CA ✓  6. C C ✓  7. A ✓  8. CA ✓  9. CA ✓  10. A ✓  11. C C ✓  12. CA ✓  13. CA ✓  14. C C ✓  15. A ✓  16. CA ✓</p>	<p>S 3: 1. C C , #1 ✓  2. BAS , #1 ✓  3. , #1 ✓  4. C C , #1 ✓  5. C C , #2 ✓  6. BAS , #2 ✓  7. , #2 ✓  8. C C , #2 ✓  9. C C , #3 ✓  10. BAS , #3 ✓  11. , #3 ✓  12. C C , #3 ✓  13. C C , #4 ✓  14. BAS , #4 ✓  15. , #4 ✓  16. C C , #4 ✓</p>	<p>S 4: 1. C C , #1 ✓  2. C C , #1 ✓  3. C C , #2 ✓  4. C C , #2 ✓  5. C C , #3 ✓  6. C C , #3 ✓  7. C C , #4 ✓  8. C C , #4 ✓  9. BAS , #4 ✓  10. , #4 ✓  11. BAS , #3 ✓  12. BAS , #3 ✓  13. BAS , #2 ✓  14. BAS , #2 ✓  15. BAS , #1 ✓  16. , #1 ✓</p>
<p>S 5: 1. A , #1 ✓  2. A , #1 ✓  3. A , #2 ✓  4. A , #2 ✓  5. A , #3 ✓  6. A , #3 ✓  7. A , #4 ✓  8. A , #4 ✓  9. A , #4 ✓  10. S C , #4 ✓  11. A , #3 ✓  12. S C , #3 ✓  13. A , #2 ✓  14. S C , #2 ✓  15. A , #1 ✓  16. S C , #1 ✓</p>	<p>S 6: 1. CA ✓  2. CA ✓  3. CA ✓  4. CA ✓  5. CA ✓  6. CA ✓  7. CA ✓  8. CA ✓  9. A ✓  10. A ✓  11. A ✓  12. A ✓  13. A ✓  14. A ✓  15. A ✓  16. A ✓</p>	<p>S 7: 1. S C -C ✓  2. C A ( ) ✓  3. C A ( ) ✓  4. A -C ✓  5. C A ( ) ✓  6. C A ( ) ✓  7. C A ( ) ✓  8. S C -C ✓  9. S C -C ✓  10. C A ( ) ✓  11. C A ( ) ✓  12. C A ( ) ✓  13. A -C ✓  14. C A ( ) ✓  15. C A ( ) ✓  16. S C -C ✓</p>	

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<b>DESCRIPTION:</b>	SOIC-16 9.90X3.90X1.50 1.27P	<b>PAGE 2 OF 2</b>

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