MC14007UB

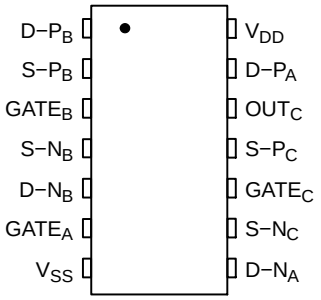
Dual Complementary Pair Plus Inverter

The MC14007UB multipurpose device consists of three N−Channel and three P−Channel enhancement mode devices packaged to provide access to each device. These versatile parts are useful in inverter circuits, pulse−shapers, linear amplifiers, high input impedance amplifiers, threshold detectors, transmission gating, and functional gating.

Features

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Pin−for−Pin Replacement for CD4007A or CD4007UB
- This device has 2 outputs without ESD Protection. Antistatic precautions must be taken.
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This Device is Pb−Free and is RoHS Compliant

PIN ASSIGNMENT



D = DRAIN
S = SOURCE

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8 second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: “D/DW” Package: –7.0 mW/°C from 65°C 5o 125°C.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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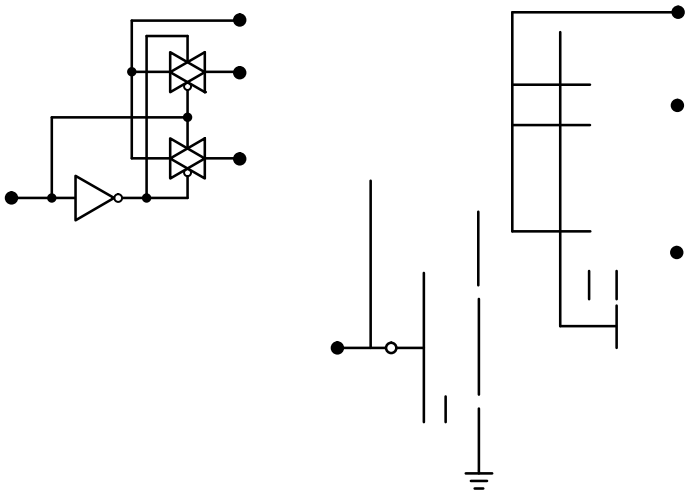
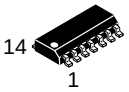


Figure 1. Typical Application: 2−Input Analog Multiplexer

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
t_{TLH}	Output Rise Time					ns
	t_{TLH} = (1.2 ns/pF) C_L + 30 ns	5.0	–	90	180	
	t_{TLH} = (0.5 ns/pF) C_L + 20 ns	10	–	45	90	
	t_{TLH} = (0.4 ns/pF) C_L + 15 ns	15	–	35	70	
t_{THL}	Output Fall Time					ns
	t_{THL} = (1.2 ns/pF) C_L + 15 ns	5.0	–	75	150	
	t_{THL} = (0.5 ns/pF) C_L + 15 ns	10	–	40	80	
	t_{THL} = (0.4 ns/pF) C_L + 10 ns	15	–	30	60	
t_{PLH}	Turn−Off Delay Time					ns
	t_{PLH} = (1.5 ns/pF) C_L + 35 ns	5.0	–	60	125	
	t_{PLH} = (0.2 ns/pF) C_L + 20 ns	10	–	30	75	
	t_{PLH} = (0.15 ns/pF) C_L + 17.5 ns	15	–	25	55	
t_{PHL}	Turn−On Delay Time					ns
	t_{PHL} = (1.0 ns/pF) C_L + 10 ns	5.0	–	60	125	
	t_{PHL} = (0.3 ns/pF) C_L + 15 ns	10	–	30	75	
	t_{PHL} = (0.2 ns/pF) C_L + 15 ns	15	–	25	55	

Figure 5. Switching Time and Power Dissipation Test Circuit and Waveforms



SCALE 1:1

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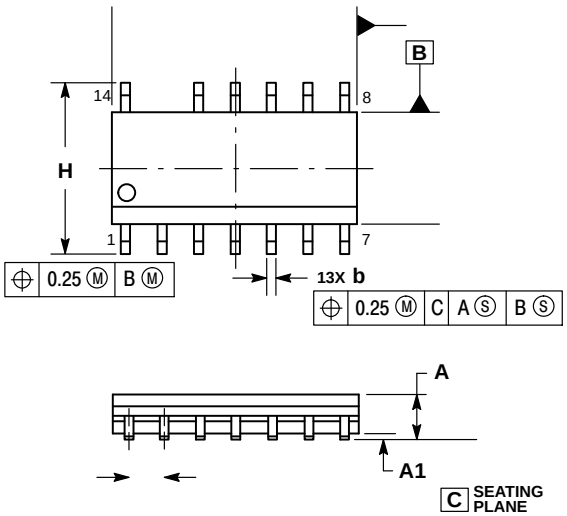
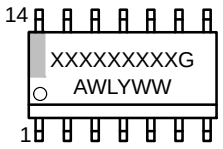


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

GENERIC
MARKING DIAGRAM*



XXXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

STYLES ON PAGE 2

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STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE

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