ON Semiconductor

http://onsemi.com

- Supply Voltage 4.5 to 5.5 V
- Low Power 3.7 mA Typical at V_{CC} = 5.0 V
- Operating Temperature Range of −40 to 85°C
- These Devices are Pb−Free and are RoHS Compliant

Table 1. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage, Pin 2	V_{CC}	0.5 to 7.0	Vdc
Operating Temperature Range	T_A	40 to 85	°C
Storage Temperature Range	T_{stg}	65 to 150	°C
Maximum Output Current, Pin 4	I_O	10	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

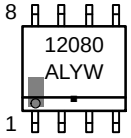
Table 2. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 1500 V > 100 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V 0 @ 0.125 in
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

MARKING DIAGRAM

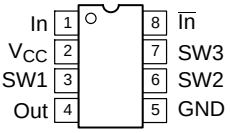
SOIC−8
D SUFFIX
CASE 751



on page 3 of th

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb Free Package

PIN CONNECTIONS



(Top View)

FUNCTION TABLE

SW1	SW2	SW3	Divide Ratio
L	L	L	80
L	L	H	40
L	H	L	40
L			20

ORDERING INFORMATION

Table 3. ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V; T_A = 40 to 85°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave)	ft	0.1	1.4	1.1	GHz
Supply Current Output (Pin 2)	I_{CC}		3.7	5.0	mA
Input Voltage Sensitivity 100 to 250 MHz 250 to 1100 MHz	V_{in}	 400 100		 1000 1000	mVpp
Divide Ratio Control Input High (SW1, SW2, SW3)	V_{IH}	V_{CC} 0.5 V	V_{CC}	V_{CC} + 0.5 V	V
Divide Ratio Control Input Low (SW1, SW2, SW3)	V_{IL}	Open	Open	Open	
Output Voltage Swing (Note 1) R_L = 820 Ω, I_O = 4.0 mA for ÷10 R_L = 1.6 kΩ, I_O = 2.1 mA for ÷20 R_L = 3.3 kΩ, I_O = 1.1 mA for ÷40 R_L = 6.2 kΩ, I_O = 0.57 mA for ÷80	V_{out}	0.8	1.2		V_{pp}

1. Assumes 8.0 pF load and 1.1 GHz input frequency (typical), I_O at V_{CC} = 5.0 V and T_A = 25°C.

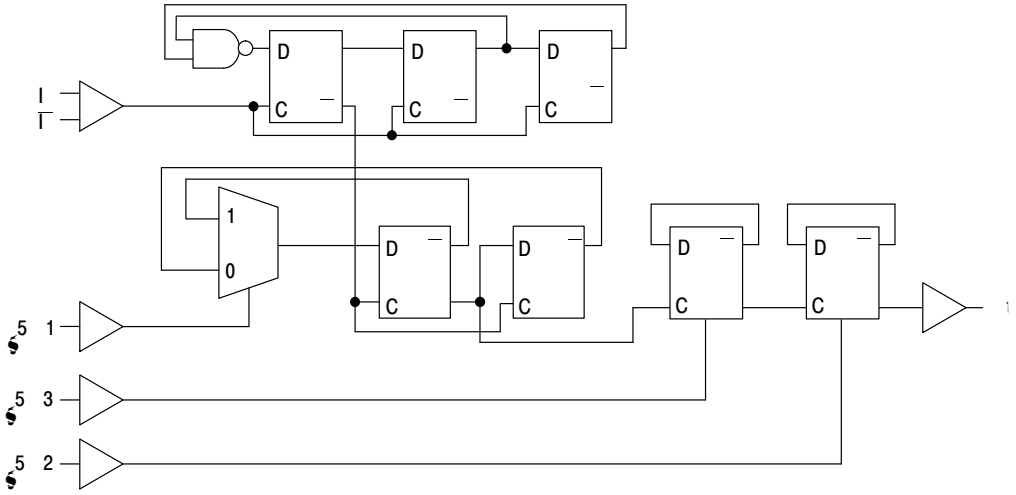


Figure 1. Logic Diagram

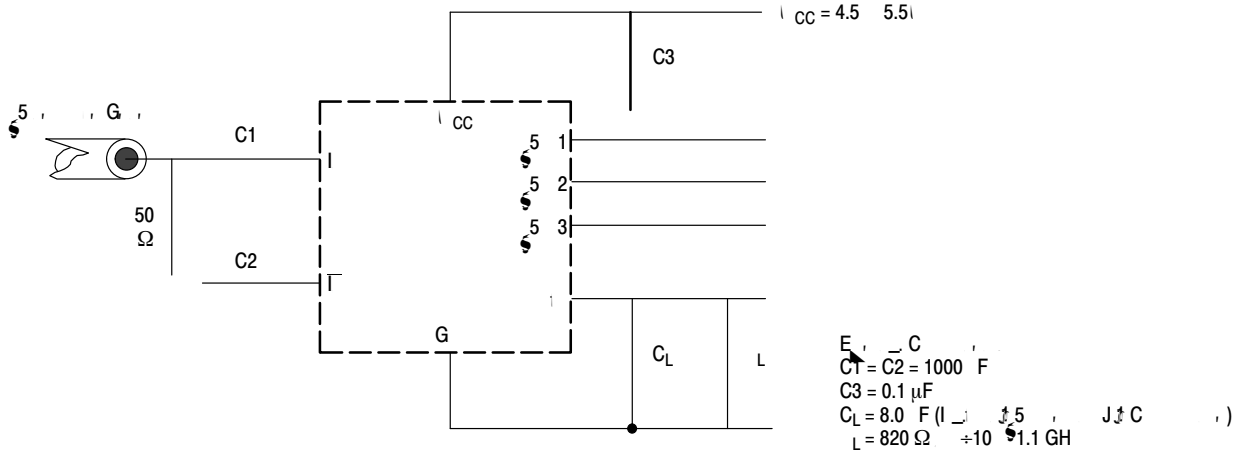


Figure 2. AC Test Circuit

–X–

– – –

⊕	0.	(0.010) Ⓜ	Ⓜ

–Y–

– – –

G

–Z–

C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0	8	0	8
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

0. (0.010) Ⓜ 1 0 1 1 0 0 1 . 0 0 0 0 . 1 1 0 1 1 . 1 0 . 0 0 0 1 . 1 1 0 0 1 1 0 ( ) 0 1 . 1 1 0 0 1 1 . 1 1 . 1 0 0 . 0 0 0 . 1 1 . 1 0 0 . 0 0 . 0 1 1 . 1 0 0 . 0 1 0 0 0 .)