▪ = Pb-Free Package

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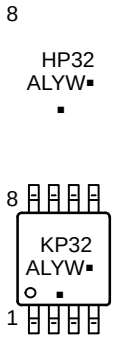
SOIC 8 NB
D SUFFIX
CASE 751 07

TSSOP 8
DT SUFFIX
CASE 948R 02

MARKING DIAGRAMS*



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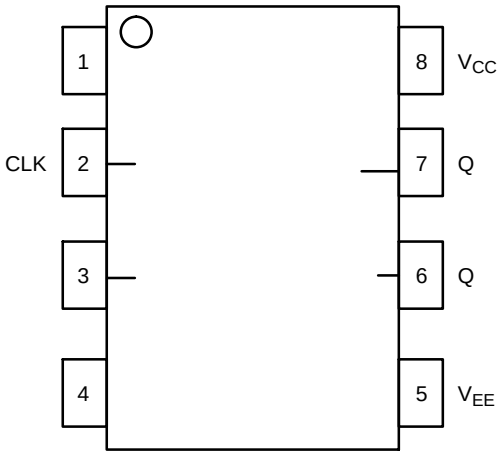

Figure 1. 8-Lead Pinout (Top View) **and Logic Diagram**

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating

Table 6. 10EP DC CHARACTERISTICS, PECL (V_{CC} = 5.0 V, V_{EE} = 0 V (Note 1))

Symbol	Characteristic	40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	23	30	40	23	30	40	23	30	40	mA
V_{OH}	Output HIGH Voltage (Note 2)	3865	3990	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 2)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3065		3390	3130		3455	3190		3515	mV
V_{BB}	Output Voltage Reference	3490	3590	3690	3555	3655	3755	3615	3715	3815	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150							

Table 8. 100EP DC CHARACTERISTICS, PECL (V_{CC} = 3.3 V, V_{EE} = 0 V (Note 1))

Symbol	Characteristic	40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	23	30	37	26	34	40	28	36	42	mA
V_{OH}	Output HIGH Voltage (Note 2)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 2)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV

V

Table 10. 100EP DC CHARACTERISTICS, NECL (V_{CC} = 0 V; V_{EE} = −5.5 V to −3.0 V (Note 1))

Symbol	Characteristic	40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	23	30	37	26	34	40	28	36	42	mA
V_{OH}	Output HIGH Voltage (Note 2)	−1145	−1020	−895	−1145	−1020	−895	−1145	−1020	−895	mV
V_{OL}	Output LOW Voltage (Note 2)	−1945	−1820	−1695	−1945	−1820	−1695	−1945	−1820	−1695	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	−1225		−880	−1225		−880	−1225		−880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	−1945		−1625	−1945		−1625	−1945		−1625	mV
V_{BB}	Output Voltage Reference	−1525	−1425	−1325	−1525	−1425	−1325	−1525	−1425	−1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150							

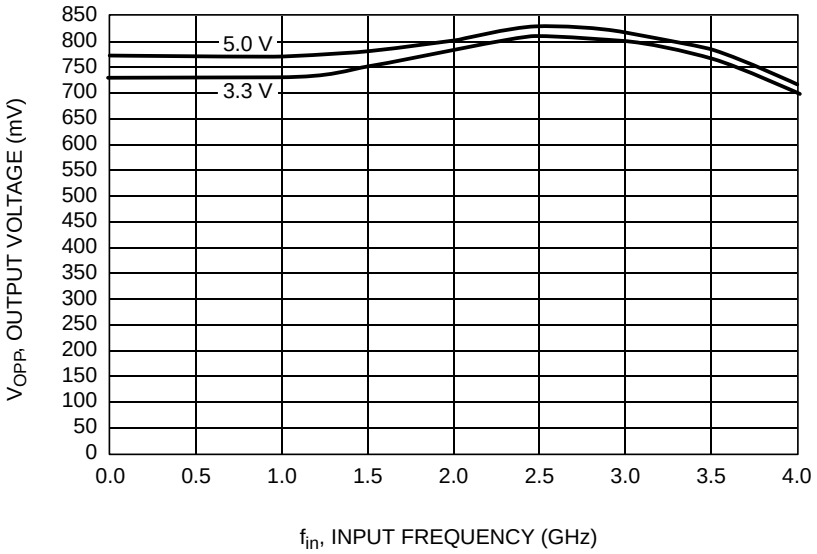

Figure 3. Input Frequency (f_{in}) Versus Typical Output Voltage (V_{OPP})

ORDERING INFORMATION

Device	Package	Shipping†
MC10EP32DG	SOIC−8 NB (Pb-Free)	98 Units / Tube
MC10EP32DR2G	SOIC−8 NB (Pb-Free)	2500 / Tape & Reel
MC10EP32DTG	TSSOP−8 (Pb-Free)	100 Units / Tube
MC10EP32DTR2G	TSSOP−8 (Pb-Free)	2500 / Tape & Reel
MC100EP32DG	SOIC−8 NB (Pb-Free)	98 Units / Tube
MC100EP32DR2G	SOIC−8 NB (Pb-Free)	2500 / Tape & Reel
MC100EP32DTG	TSSOP−8 (Pb-Free)	100 Units / Tube
MC100EP32DTR2G	TSSOP−8 (Pb-Free)	2500 / Tape & Reel
MC100EP32MNR4G	DFN−8 (Pb-Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

DFN8 2x2, 0.5P
CASE 506AA
ISSUE F

DATE 04 MAY 2016

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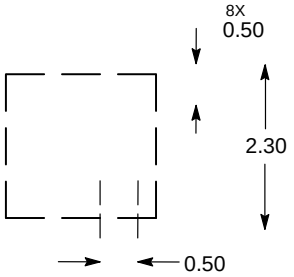
SCALE 4:1

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

–X–

– – –

⊕	0.	(0.010) Ⓜ	Ⓜ

–Y–

– – –

G

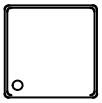
–Z–

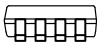
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0	8	0	8
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

0. (0.010) Ⓜ 1 0 1 1 0 0 1 . 0 0 0 0 . 1 1 0 1 1 . 1 0 . 0 0 0 1 . 1 1 0 0 1 1 0 ( ) 0 1 . 1 1 0 0 1 1 . 1 1 . 1 0 0 . 0 0 0 . 1 1 . 1 0 0 . 0 0 . 0 1 1 . 1 0 0 . 0 1 0 0 0 .)

TSSOP 8
CASE 948R−02
ISSUE A

DATE 04/07/2000





	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A				