3.3 V /5 V ÷2/4, ÷4/5/

10 13 , 100 13

Description

The MC10/100EP139 is a low skew ÷2/4, ÷4/5/6 clock generation chip

10 0 0 10 313.053 3 34.6615 Tm-.0227Tc.1628Tw(via)-22.7)29(a)]TJ25.3304 -1.207 TD-.0237Tc0 Tw(0.01)TjF3 1 Tf1.65 0 TD0 Tc()

MC10EP139DTG	TSSOP−20 WB (Pb-Free)

April, 2021 − Rev. 15
Publication Order Number:
MC10EP139/D

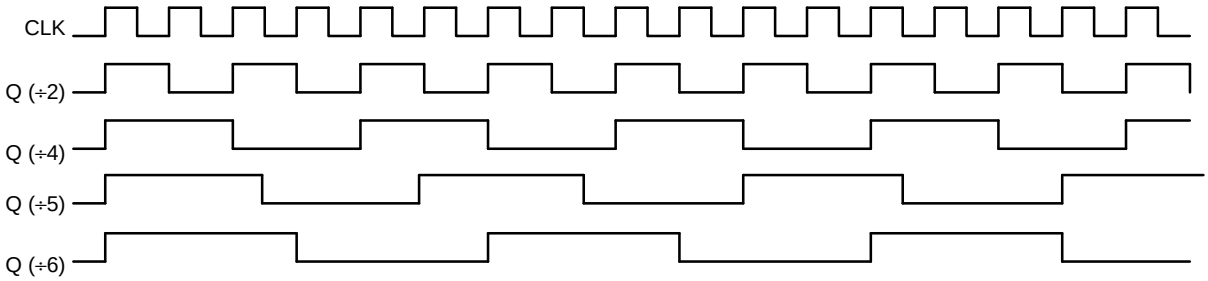

Figure 3. CLK and OUTPUT Timing Diagram

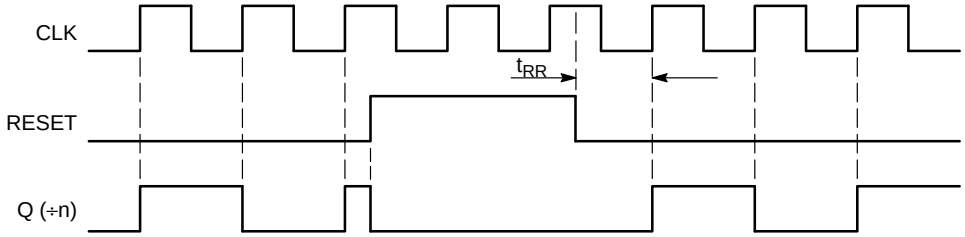

Figure 4. Timing Diagram

Table 3. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 kΩ
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	 > 2 kV > 100 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb-Free Pkg
SOIC−20 WB TSSOP−20 W	Level 3 Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count	

Table 5. 10EP DC CHARACTERISTICS, PECL (V_{CC} = 3.3 V, V_{EE} = 0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	65	82	105	65	83	105	65	84	105	mA
V_{OH}	Output HIGH Voltage (Note 2)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 2)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1365		1690	1460		1755	1490		1815	mV
V_{BB}	Output Voltage Reference	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5									

Table 7. 10EP DC CHARACTERISTICS, NECL (V_{CC} = 0 V, V_{EE} = −5.5 V to −3.0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	65	82	105	65	83	105	65	84	105	mA

Table 11. AC CHARACTERISTICS (V_{CC} = 0 V; V_{EE} = −3.0 V to −5.5 V or V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0 V (Note 1))

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Frequency TEee H2.8709 Tmrres 5, 6, 7 and535F0 0 6.5 215.263 7907.91666797.1422 Tc(max)TJMax										

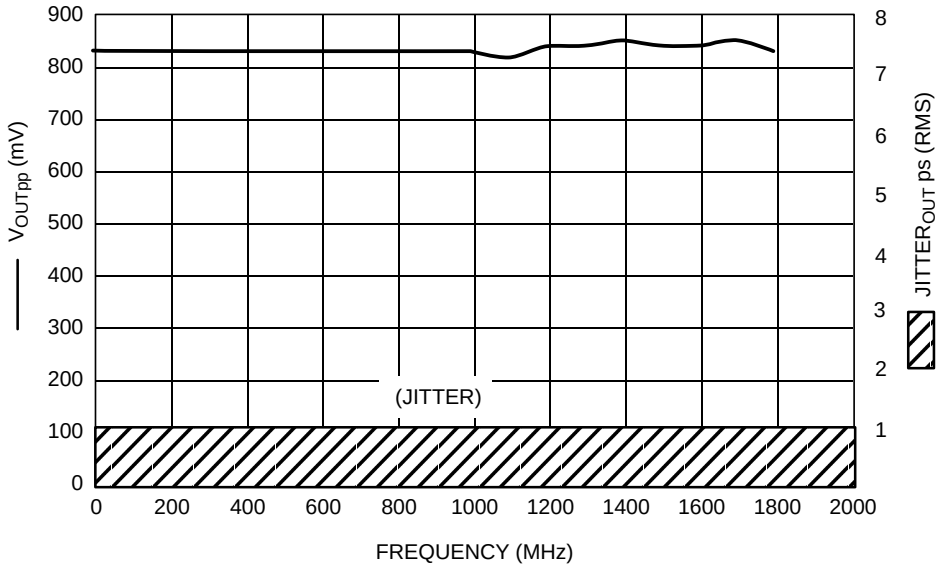

Figure 5. ÷2, F_{max}/Jitter

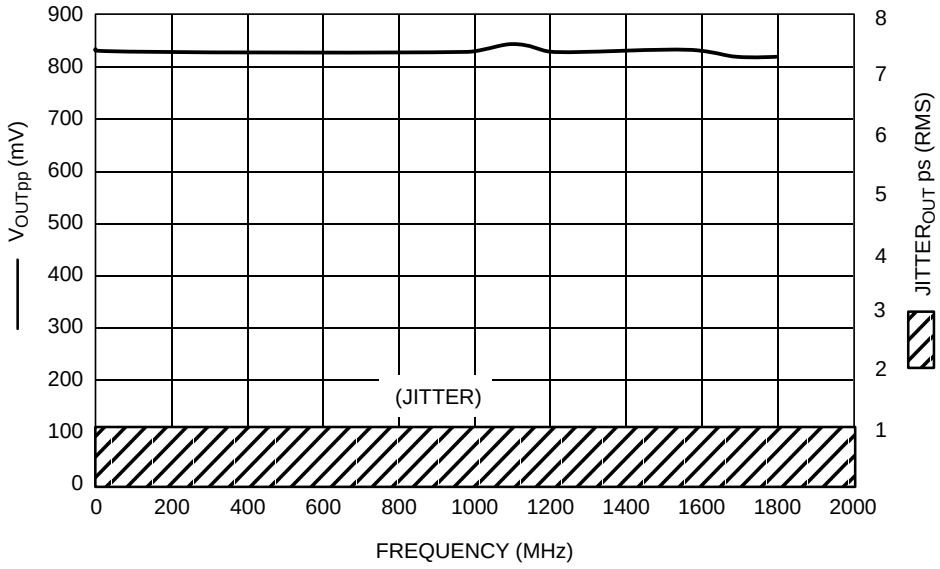

Figure 6. ÷5, F_{max}/Jitter

Resource Reference of Application Notes

AN1405/D − ECL Clock Distribution Techniques

AN1406/D − Designing with PECL (ECL at +5.0 V)

AN1503/D − ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D − Metastability and the ECLinPS Family

AN1568/D − Interfacing Between LVDS and ECL

AN1672/D − The ECL Translator Guide

AND8001/D − Odd Number Counters Design

AND8002/D − Marking and Date Codes

AND8020/D − Termination of ECL Logic Devices

AND8066/D − Interfacing with ECLinPS

AND8090/D − AC Characteristics of ECL Devices

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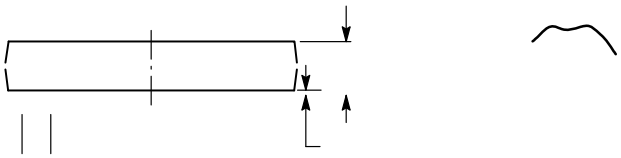

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