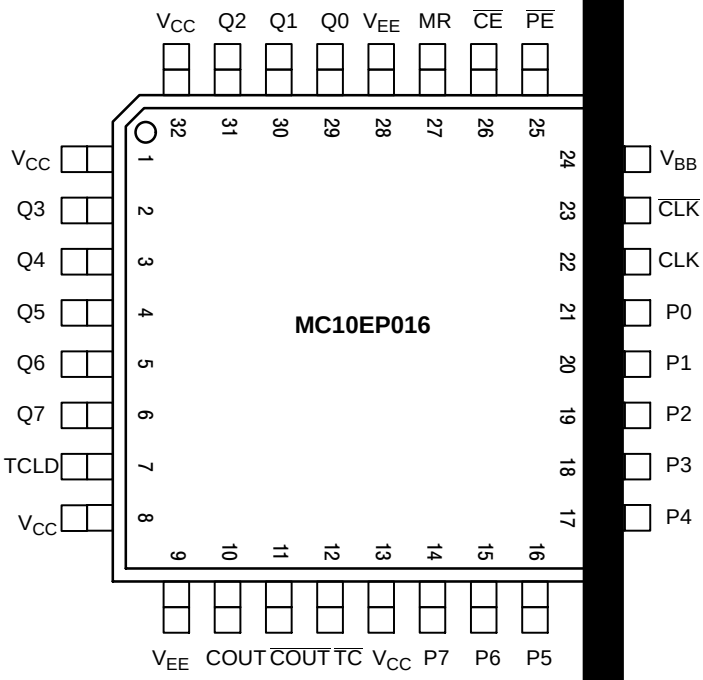


Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. LQFP−32 Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin	Function
P0−P7*	ECL Parallel Data (Preset) Inputs
Q0−Q7	ECL Data Outputs
$\overline{CE}$*	ECL Count Enable Control Input
$\overline{PE}$*	ECL Parallel Load Enable Control Input
MR*	ECL Master Reset
CLK*, $\overline{CLK}$*	ECL Differential Clock
$\overline{TC}$	ECL Terminal Count Output

$\overline{CE}$	FUNCTION
X	
L	
L	
H	
X	
X	

ZZ = Clock Pulse (High−to−Low)
Z = Clock Pulse (Low−to−High)

Table 5. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		6	

Table 6. 10EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 3)

Table 8. 10EP DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = −5.5 V to −3.0 V (Note 10)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current (Note 11)	120	160	200	120	160	200	120	160	200	mA
V_{OH}	Output HIGH Voltage (Note 12)	−1135	−1010	−885	−1070	−945	−820	−1010	−885	−760	mV
V_{OL}	Output LOW Voltage (Note 12)	−1935	−1810	−1685	−1870	−1745	−1620	−1810	−1685	−1560	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	−1210		−885	−1145		−820	−1085		−760	mV
V_{IL}	Input LOW Voltage (Single−Ended)	−1935		−1610	−1870		−1545	−1810		−1485	mV
V_{BB}	Output Voltage Reference	−1510	−1410	−1310	−1445	−1345	−1245	−1385	−1285	−1185	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

10. Input and output parameters vary 1:1 with V_{CC}.
11. Required 500 lfpm air flow when using −5 V power supply. For (V_{CC} − V_{EE}) >3.3 V, 5 Ω to 10 Ω in line with V_{EE} required for maximum thermal protection at elevated temperatures. Recommend V_{CC}−V_{EE} operation at $\leq$ 3.3 V.
12. All loading with 50 Ω to V_{CC} − 2.0 V.
13. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 9. AC CHARACTERISTICS V_{EE} = −3.0 V to −5.5 V; V_{CC} = 0 V or V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0 V (Note 14)

		−40°C	25°C	85°C

APPLICATIONS INFORMATION

Cascading Multiple EP016 Devices

For applications which call for larger than 8−bit counters multiple EP016s can be tied together to achieve very wide bit width counters. The active low terminal count ($\overline{TC}$) output and count enable input ($\overline{CE}$) greatly facilitate the cascading of EP016 devices. Two EP016s can be cascaded without the need for external gating, however for counters wider than 16 bits external OR gates are necessary for cascade implementations.

Figure 3 below pictorially illustrates the cascading of 4 EP016s to build a 32−bit high frequency counter. Note the EP01 gates used to OR the terminal count outputs of the lower order EP016s to control the counting operation of the higher order bits. When the terminal count of the preceding device (or devices) goes low (the counter reaches an all 1s state)

APPLICATIONS INFORMATION (CONTINUED)

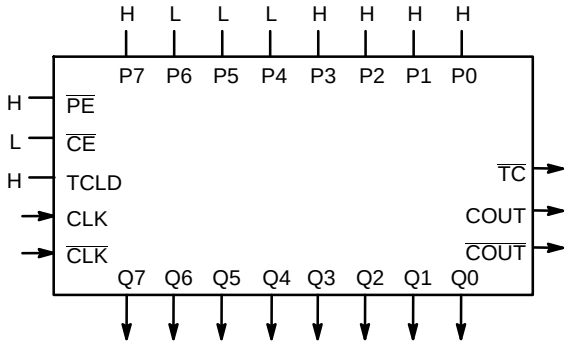


Figure 4. Mod 2 to 256 Programmable Divider

To determine what value to load into the device to accomplish the desired division, the designer simply subtracts the binary equivalent of the desired divide ratio from the binary value for 256. As an example for a divide ratio of 113:

Pn's = 256 − 113 = $8F_{16}$ = 1000 1111

where:

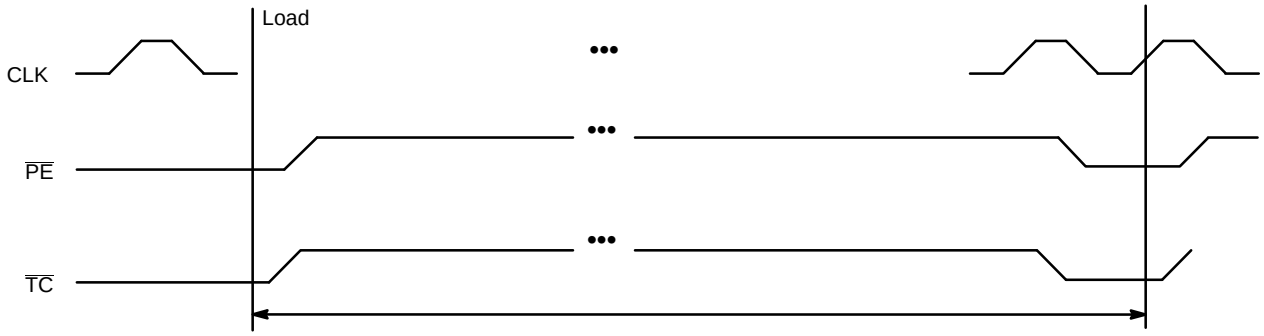
P0 = LSB and P7 = MSB

Forcing this input condition as per the setup in Figure 4 will result in the waveforms of Figure 5. Note that the $\overline{TC}$ output is used as the divide output and the pulse duration is equal to a full clock period. For even divide ratios, twice the desired divide ratio can be loaded into the EP016 and the $\overline{TC}$ output can feed the clock input of a toggle flip flop to create a signal divided as desired with a 50% duty cycle.

Table 10. PRESET VALUES FOR VARIOUS DIVIDE RATIOS

Divide Ratio	Preset Data Inputs							
	P7	P6	P5	P4	P3	P2	P1	P0
2	H	H	H	H	H	H	H	L
3	H	H	H	H	H	H	L	H
4	H	H	H	H	H	H	L	L
5	H	H	H	H	H	L	H	H
w	w	•	•	•	•	•	•	•
w	•	•	•	•	•	•	•	•
112	H	L	L	H	L	L	L	L
113	H	L	L	L	H	H	H	H
114	H	L	L	L	H	H	H	L
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
254	L	L	L	L	L	L	H	L
255	L	L	L	L	L	L	L	H
256	L	L	L	L	L	L	L	L

A single EP016 can be used to divide by any ratio from 2 to 256 inclusive. If divide ratios of greater than 256 are needed multiple EP016s can be cascaded in a manner similar to that already discussed. When EP016s are cascaded to build larger dividers the TCLD pin will no longer provide a means for loading on terminal count. Because one does not want to reload the counters until all of the devices in the chain have reached terminal count, external gating of the $\overline{TC}$ pins must be used for multiple EP016 divider chains.



ORDERING INFORMATION

Device	Package	Shipping†
MC10EP016FAG	LQFP−32 (Pb−Free)	250 Units / Tray
MC10EP016FAR2G	LQFP−32 (Pb−Free)	2,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D − ECL Clock Distribution Techniques

AN1406/D − Designing with PECL (ECL at +5.0 V)

AN1503/D − ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D − Metastability and the ECLinPS Family

AN1568/D − Interfacing Between LVDS and ECL

AN1672/D − The ECL Translator Guide

AND8001/D − Odd Number Counters Design

AND8002/D − Marking and Date Codes

AND8020/D − Termination of ECL Logic Devices

AND8066/D − Interfacing with ECLinPS

AND8090/D − AC Characteristics of ECL Devices