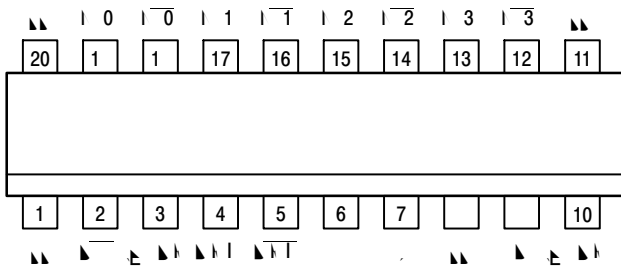


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Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Pinout: SOIC-20 WB (Top View)

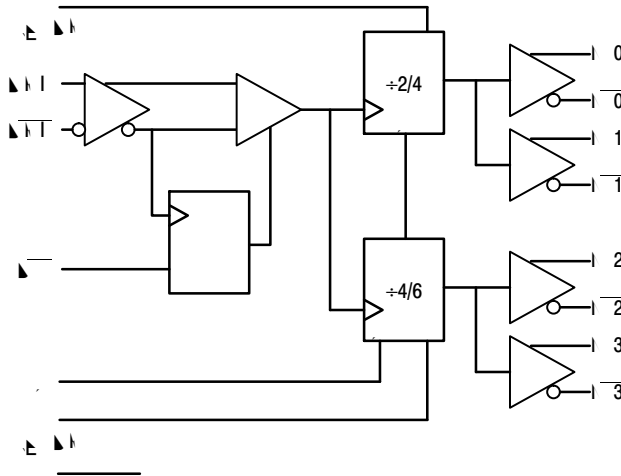


Figure 2. Logic Diagram

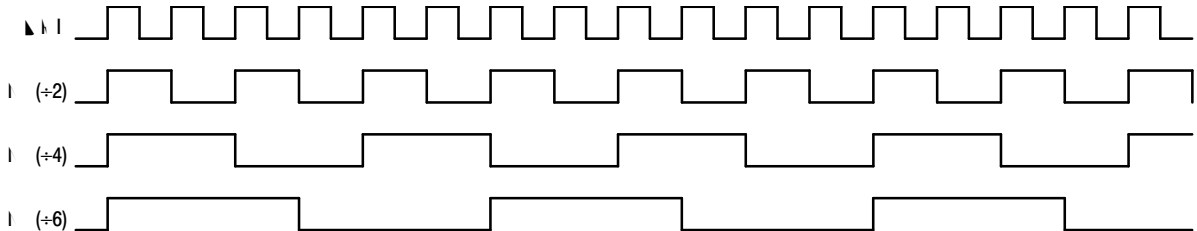


Figure 3. Timing Diagrams

Table 1. PIN DESCRIPTION

Column Head	
CLK, $\overline{\text{CLK}}$	ECL Diff Clock Inputs
$Q_0, Q_1; \overline{Q_0}, \overline{Q_1}$	ECL Diff $\pm 2/4$ Outputs
$Q_2, Q_3; \overline{Q_2}, \overline{Q_3}$	ECL Diff $\pm 4/6$ Outputs
DIVSEL _a , DIVSEL _b	ECL Frequency Select Inputs
EN	ECL Sync Enable
MR	ECL Master Reset
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

Table 2. FUNCTION TABLE

CLK	EN	MR	Function
Z	L	L	Divide
ZZ	H	L	Hold Q_0-3
X	X	H	Reset Q_0-3

Z = Low-to-High Transition
 ZZ = High-to-Low Transition
 X = Don't Care

DIVSEL _a	Q_0, Q_1 Outputs
L	Divide by 2
H	Divide by 4

DIVSEL _b	Q_2, Q_3 Outputs
L	Divide by 4
H	Divide by 6

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Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		8 to 0	V
V _{EE}	NECL Mode Power Supply	V _{CC} = 0 V		-8 to 0	

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Table 5. LVNECL DC CHARACTERISTICS ($V_{CC} = 0.0\text{ V}$; $V_{EE} = -3.3\text{ V}$ (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		50	59		50	59		54	61	mA
V_{OH}	Output HIGH Voltage (Note 2)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage (Note 2)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV

V_{BB}

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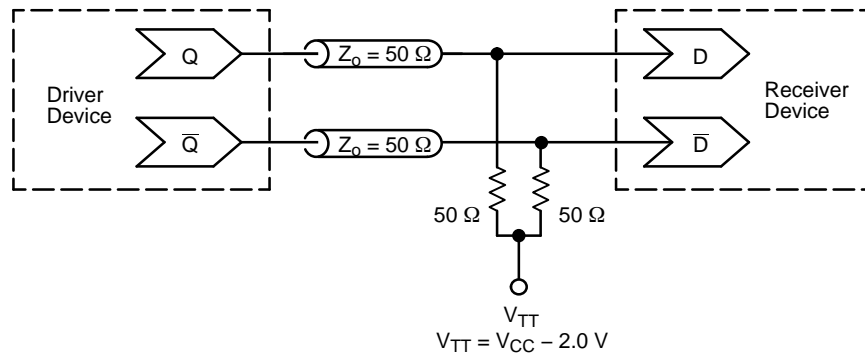


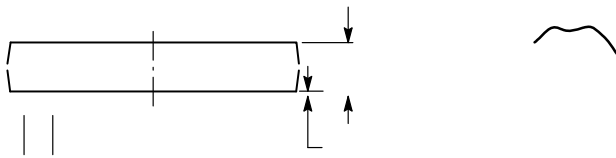
Figure 4. Typical Termination for Output Driver and Device Evaluation
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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