

## 3.3 ECL ÷2, ÷4, ÷8 C

### C100L EL34

#### Description

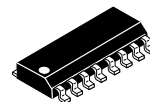
The MC100LVEL34 is a low skew ÷2, ÷4, ÷8 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

The common enable ( $\overline{EN}$ ) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock; therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon start up, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as multiple LVEL34s in a system.

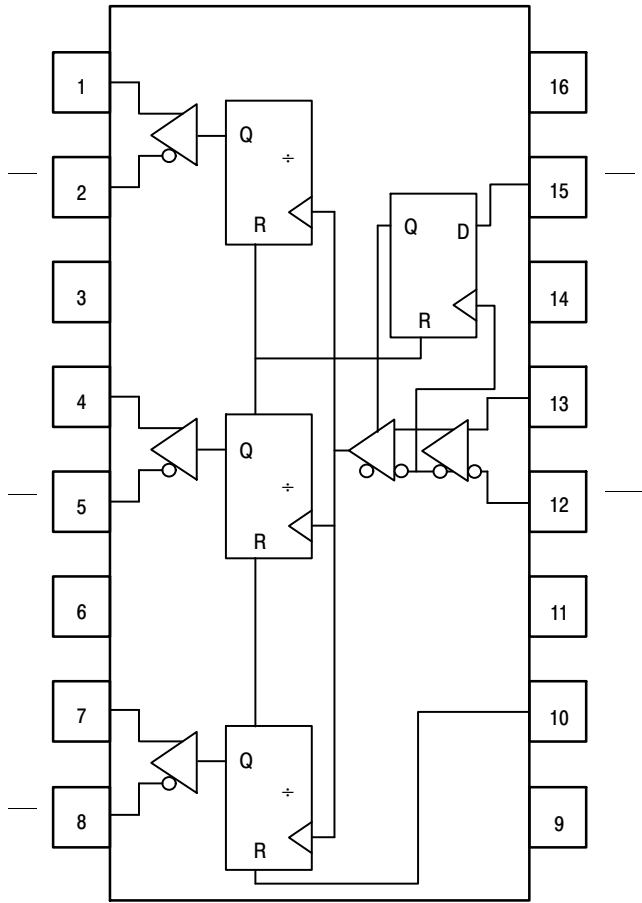
#### Features

- 50 ps Typical Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- 1.5 GHz Toggle Frequency
- The 100 Series Contains Temperature Compensation.
- PECL Mode Operating Range:  
 $V_{CC} = 3.0 \text{ V to } 3.8 \text{ V with } V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range:  
 $V_{CC} = 0 \text{ V with } V_{EE} = 3.0 \text{ V to } 3.8 \text{ V}$
- Open Input Default State
- LVDS Input Compatible
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



SOIC-16  
D SUFFIX  
CASE 751B

# MC100LEVEL34



**Table 1. PIN DESCRIPTION**

Pin	Description
1	CLK
2	D
3	EN
4	CLK
5	D
6	EN
7	CLK
8	D
9	MR
10	Q
11	Q
12	CLK
13	D
14	D
15	D
16	Q

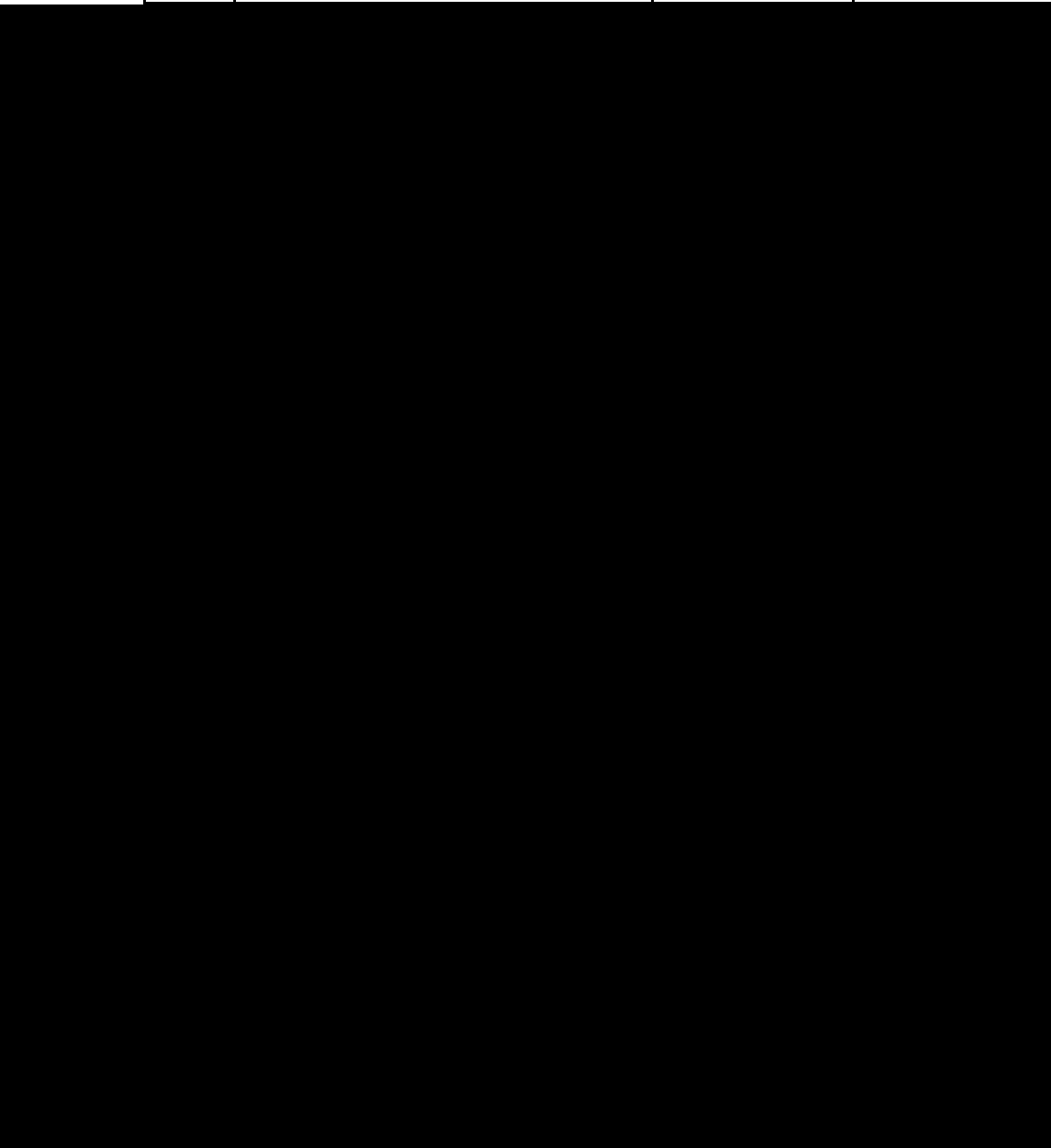
**Table 2. FUNCTION TABLE**

CLK	EN	MR	Q
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

# MC100LEVEL34

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
				-	
			$\leq$ $\geq$	-	
				$\pm$	
				-	°
				-	°
$\theta$	--		-		°
$\theta$	--		-		°
$\theta$	--		-		°
$\theta$	--		-		°
					°



85°C			Unit
Min	Typ	Max	
			$\mu$

# MC100LEVEL34

Table 6. 100LEVEL DC CHARACTERISTICS, NECL

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		-	-	-	-	-	-	-	-	-	
		-	-	-	-	4 5 7 5					

**MC100LEVEL34**





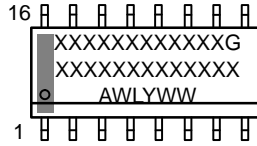
**SOIC-16 9.90x3.90x1.50 1.27P**  
CASE 751B  
ISSUE L



SOIC-16 9.90x3.90x1.50 1.27P  
CASE 751B  
ISSUE L

DATE 29 MAY 2024

GENERIC  
MARKING DIAGRAM\*



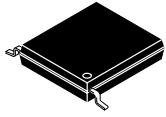
XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

<p>S 1  N 1. C C  2. BAS  3.  4. N C NW C N  5.  6. BAS  7. C C  8. C C  J. BAS  10.  11. N C NW C N  12.  13. BAS  14. C C  15.  16. C C</p>	<p>S 2  N 1. CA  2. AN  3. N C NW C N  4. CA  5. CA  6. N C NW C N  7. AN  8. CA  J. CA  10. AN  11. N C NW C N  12. CA  13. CA  14. N C NW C N  15. AN  16. CA</p>	<p>S 3  N 1. C C , #1  2. BAS , #1  3. , #1  4. C C , #1  5. C C , #2  6. BAS , #2  7. , #2  8. C C , #2  J. C C , #3  10. BAS , #3  11. , #3  12. C C , #3  13. C C , #4  14. BAS , #4  15. , #4  16. C C , #4</p>	<p>S 4  N 1. C C , #1  2. C C , #1  3. C C , #2  4. C C , #2  5. C C , #3  6. C C , #3  7. C C , #4  8. C C , #4  J. BAS , #4  10. , #4  11. BAS , #3  12. , #3  13. BAS , #2  14. , #2  15. BAS , #1  16. , #1</p>
<p>S 5  N 1. AN , #1  2. AN , #1  3. AN , #2  4. AN , #2  5. AN , #3  6. AN , #3  7. AN , #4  8. AN , #4  J. A , #4  10. S C , #4  11. A , #3  12. S C , #3  13. A , #2  14. S C , #2  15. A , #1  16. S C , #1</p>	<p>S 6  N 1. CA  2. CA  3. CA  4. CA  5. CA  6. CA  7. CA  8. CA  J. AN  10. AN  11. AN  12. AN  13. AN  14. AN  15. AN  16. AN</p>	<p>S 7  N 1. S C N-C  2. C N AN ( )  3. C N AN ( )  4. A -C  5. C N AN ( )  6. C N AN ( )  7. C N AN ( )  8. S C -C  J. S C -C  10. C N AN ( )  11. C N AN ( )  12. C N AN ( )  13. A N-C  14. C N AN ( )  15. C N AN ( )  16. S C N-C</p>	

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**SCALE 2:1**

**TSSOP-16 WB**  
CASE 948F  
ISSUE B

DATE 19 OCT 2006

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