3.3 ECL ÷2, ÷4, ÷8 C i
G C

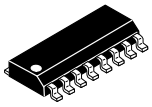
C100L EL34

Description

The MC100LVEL34 is a low skew ÷ 2, ÷ 4, ÷ 8 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock; therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon start up, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as multiple LVEL34s in a system.



SOIC−16
D SUFFIX
CASE 751B

Features

- 50 ps Typical Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- 1.5 GHz Toggle Frequency
- The 100 Series Contains Temperature Compensation.
- PECL Mode Operating Range:
  V_{CC} = 3.0 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range:
  V_{CC} = 0 V with V_{EE} = 3.0 V to 3.8 V
- Open Input Default State
- LVDS Input Compatible
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

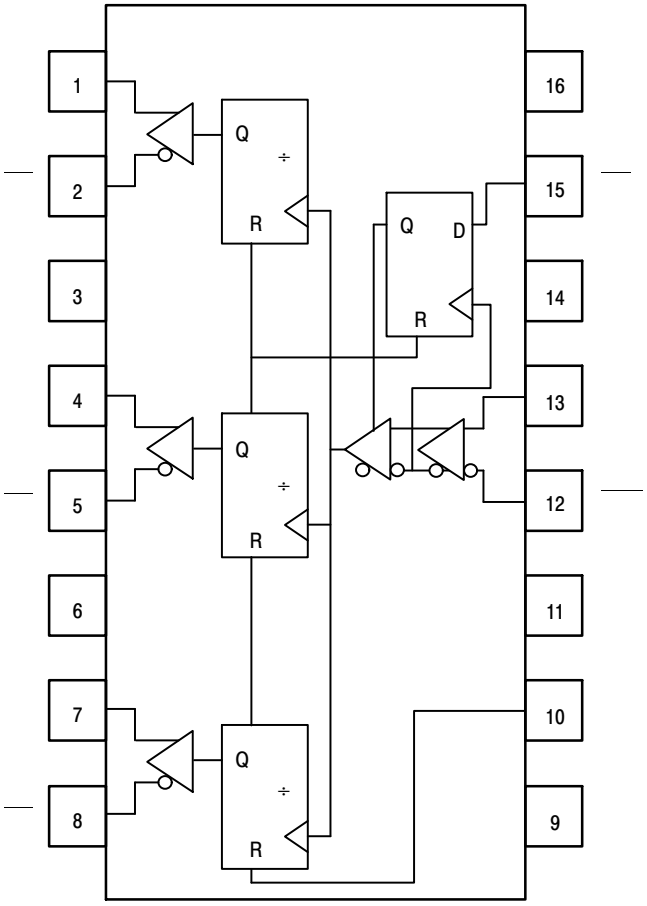


Table 1. PIN DESCRIPTION

	÷
	÷
	÷

Table 2. FUNCTION TABLE

CLK	$\overline{EN}$	MR	

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
				–	
			≤ ≥	–	
				±	
				–	°
				–	°
θ	– –		– –		° °
θ	– –		–		°
θ	– –		– –		° °
θ	– –		–		°
					°

85°C			
Min	Typ	Max	Unit
			µ

Table 6. 100LVEL DC CHARACTERISTICS, NECL – –

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		–	–	–	–	–	–	–	–	–	
		–	–	–	–	1 5 7 5					

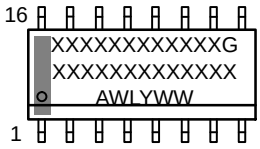
MC100LVEL34

SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

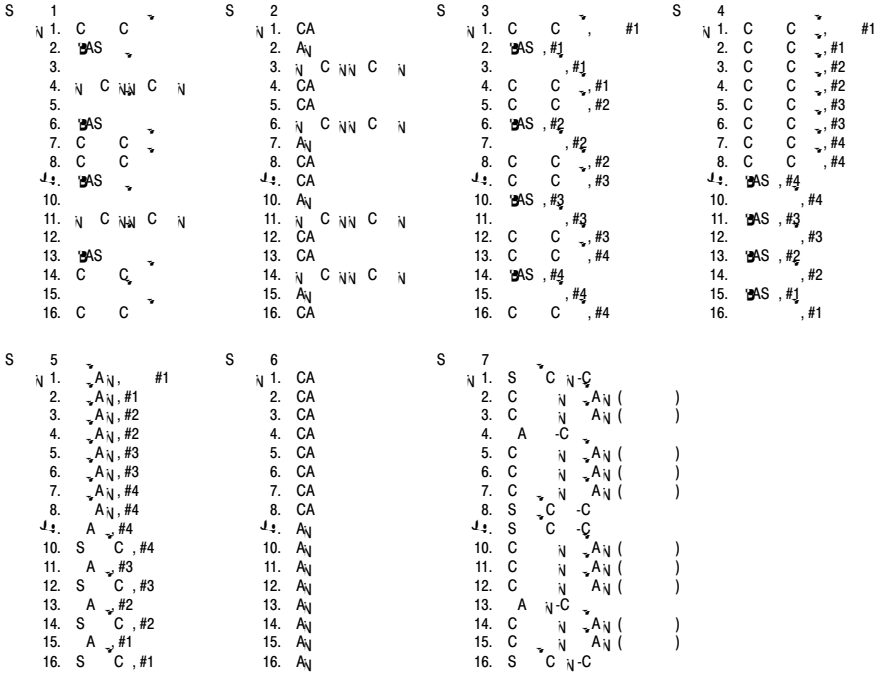
DATE 29 MAY 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



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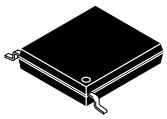

SCALE 2:1

TSSOP−16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006