

### Description

The MC100LVEL11 is a differential 1:2 fanout buffer. The device is functionally similar to the E111 device but with higher performance capabilities. Having within-device skews and output transition times significantly improved over the E111, the LVEL11 is ideally suited for those applications which require the ultimate in AC performance.

The differential inputs of the LVEL11 employ clamping circuitry to maintain stability under open input conditions. If the inputs are left open (pulled to  $V_{EE}$ ) the Q outputs will go LOW.

### Features

- 330 ps Propagation Delay
- 5 ps Skew Between Outputs
- High Bandwidth Output Transitions
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:  $V_{CC} = 3.0\text{ V}$  to  $3.8\text{ V}$  with  $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -3.0\text{ V}$  to  $-3.8\text{ V}$
- Internal Input Pulldown Resistors on D, Pullup and Pulldown Resistors on  $\bar{D}$
- Q Output will Default LOW with Inputs Open or at  $V_{EE}$
- These Devices are Pb-Free and are RoHS Compliant

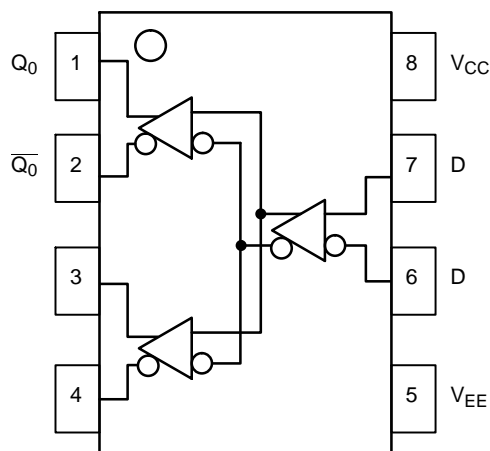


Figure 1. Logic Diagram and Pinout Assignment

# MC100LEVEL11

**Table 1. PIN DESCRIPTION**

Pin	Function
Q0, $\overline{Q0}$ ; Q1, $\overline{Q1}$	ECL Data Outputs
D, $\overline{D}$	ECL Data Inputs
V <sub>CC</sub>	Positive Supply
V <sub>EE</sub>	Negative Supply
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

**Table 2. ATTRIBUTES**

Characteristics	Value
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**Table 4. LVPECL DC CHARACTERISTICS**  $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  (Note 3)

Symbol	Characteristic	-40°C			25°C			95°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		24	28		24	28		25	30	mA
$V_{OH}$	Output HIGH Voltage (Note 4)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
$V_{OL}$	Output LOW Voltage (Note 4)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	1490		1825	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 8) $V_{pp} < 500\text{ mV}$ $V_{pp} \geq 500\text{ mV}$	1.2		3.1	1.1		3.1	1.1		3.1	V
		1.4		3.1	1.3		3.1	1.3		3.1	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	D	0.5		0.5			0.5			$\mu\text{A}$
		$\bar{D}$	-600		-600			-600			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

- Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
- Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
- $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and  $1.0\text{ V}$ .

**Table 5. LVNECL DC CHARACTERISTICS**  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 6)

Symbol	Characteristic	-40°C			25°C			95°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		24	28		24	28		25	30	mA
$V_{OH}$	Output HIGH Voltage (Note 7)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
$V_{OL}$	Output LOW Voltage (Note 7)	-1830	-1695	-1555	-1810	-1705	-1620	-1810			

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**Table 6. AC CHARACTERISTICS**  $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 9)

Symbol	Characteristic	-40°C			25°C			95°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\max}$	Maximum Toggle Frequency					1.0					GHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay to Output	235		385	255	330	405	285		435	ps
$t_{SKEW}$	Within-Device Skew (Note 10) Device-to-Device (Note 11) Duty Cycle Skew										

# MC100LEVEL11

## ORDERING INFORMATION

Device	Package	Shipping†
MC100LEVEL11DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC100LEVEL11DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC100LEVEL11DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC100LEVEL11DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC100LEVEL11MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### Resource Reference of Application Notes

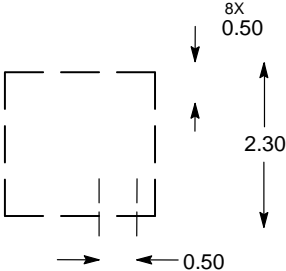
- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

**DFN8 2x2, 0.5P**  
CASE 506AA  
ISSUE F

DATE 04 MAY 2016

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SCALE 4:1

**SOLDERING FOOTPRINT\***



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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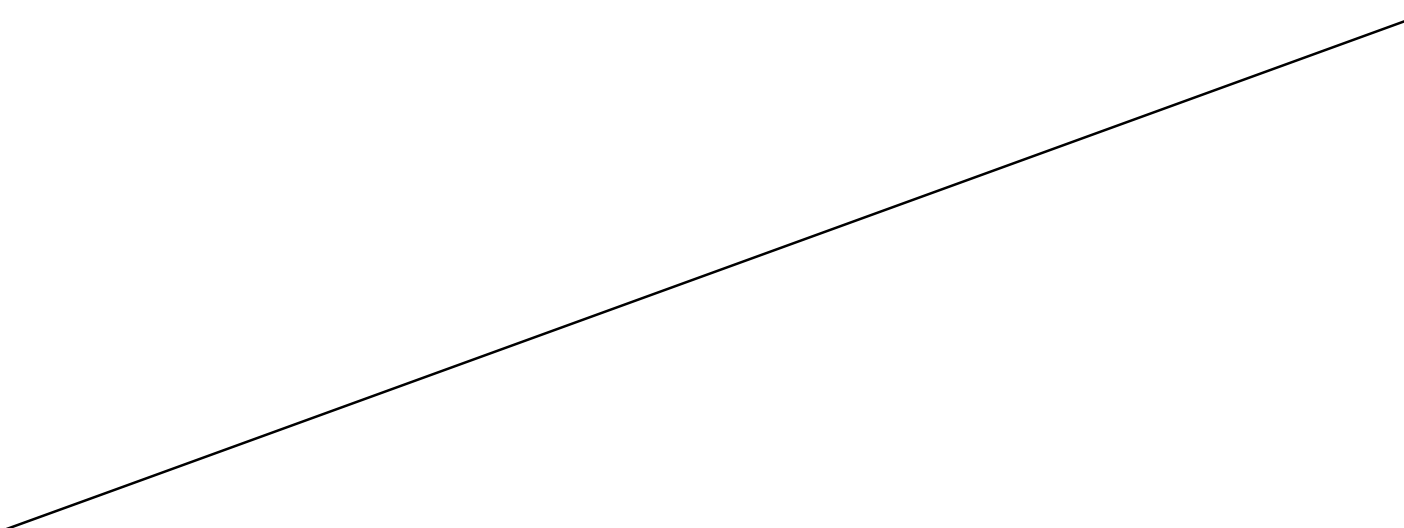
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C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0	8	0	8
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

0. (0.010) ○ 1011001.000 0.1 1011. 100 0001.1 1001 1 0( )01.1 100111.1.10000 5.80 6.20 0.228 0.244 1.0 0 1000 0. )

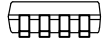
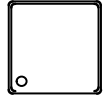






TSSOP 8  
CASE 948R-02  
ISSUE A

DATE 04/07/2000



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A				

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