3.3 V/5 V ECL 8-Bit Serial/Parallel Converter

MC100EP445

Description

The MC100EP445 is an integrated 8–bit differential serial to parallel data converter with asynchronous data synchronization. The device has two modes of operation. CKSEL HIGH mode is designed to operate NRZ data rates of up to 3.3 Gb/s, while CKSEL LOW mode5d

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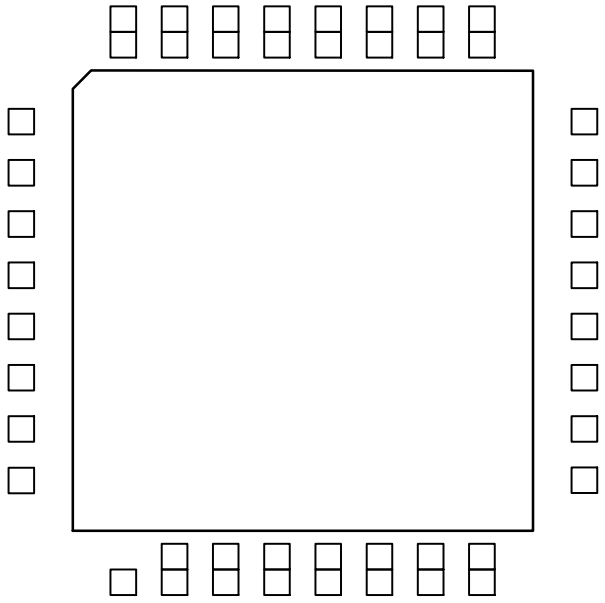
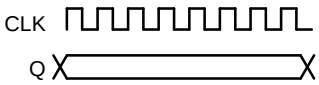
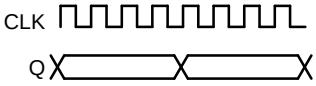

Q7

Table 2. TRUTH TABLE

PIN	FUNCTION	
	High	**Low**
SINSEL	Select SINB Input	Select SINA Input
CKSEL	Q: PCLK = 8:1 CLK: Q = 1:1 	Q: PCLK = 8:1 CLK: Q = 1:2 
$\overline{CKEN}$	Synchronously Disable Internal Clock Circuitry	Synchronously Enable Internal Clock Circuitry
RESET	Asynchronous Master Reset	Synchronous Enable
SYNC	Asynchronously Applied to Swallow a Data Bit	Normal Conversion Process

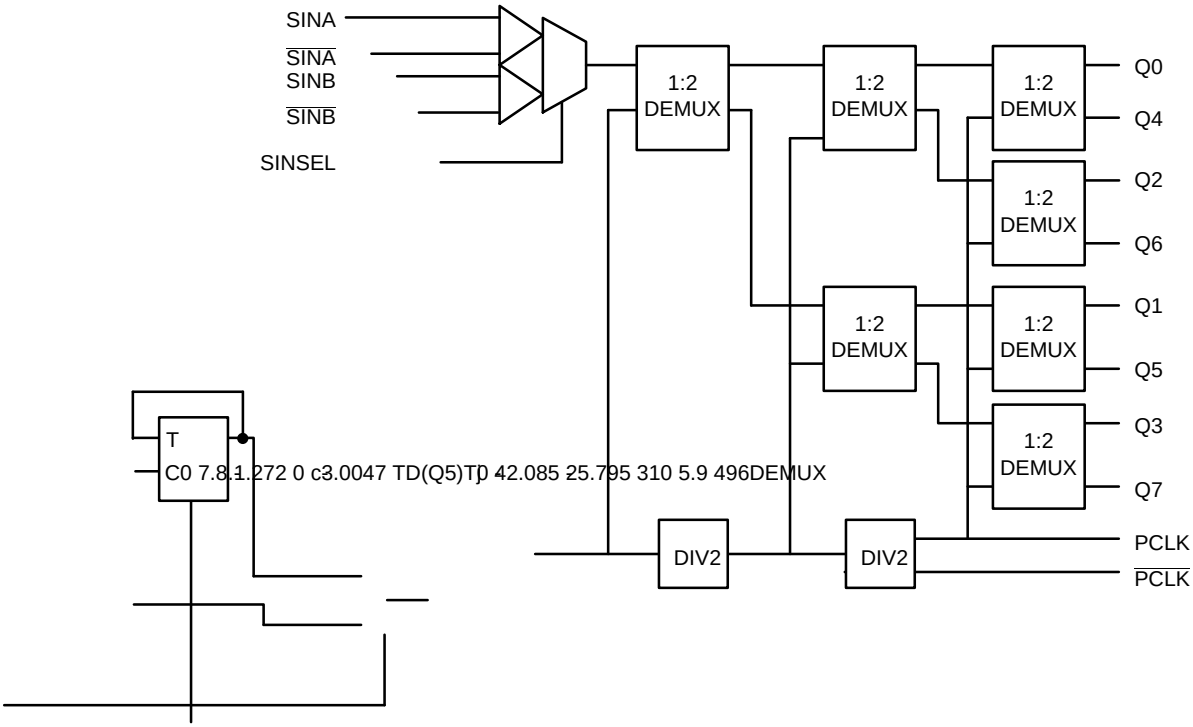


Figure 3. Logic Diagram

Table 3. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 kΩ
Internal Input Pull−up Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	 > 2 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb−Free Pkg
LQFP−32 QFN−32	Level 2 Level 1
Flammability Rating Oxygen Index: 28 to 34	 UL 94 V−0 @ 0.125 in
Transistor Count	993 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		−6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 −6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			±0.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction				

Table 5. 100EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 2)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	95	119	143	98	122	146	100	125	150	mA
$V_{OH=}$											

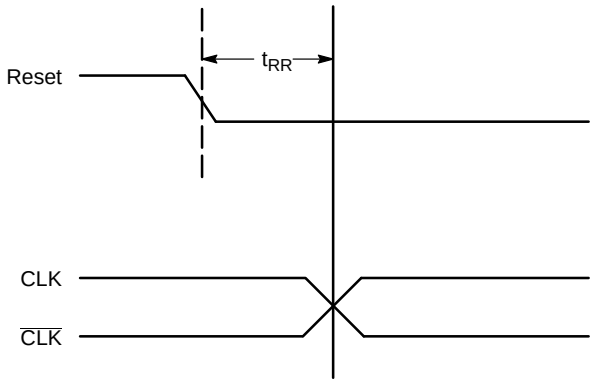


Figure 4. Reset Recovery

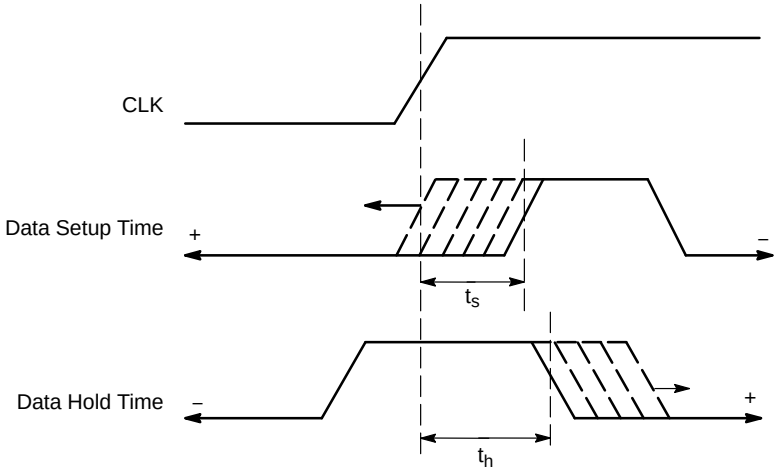


Figure 5. Data Setup and Hold Time

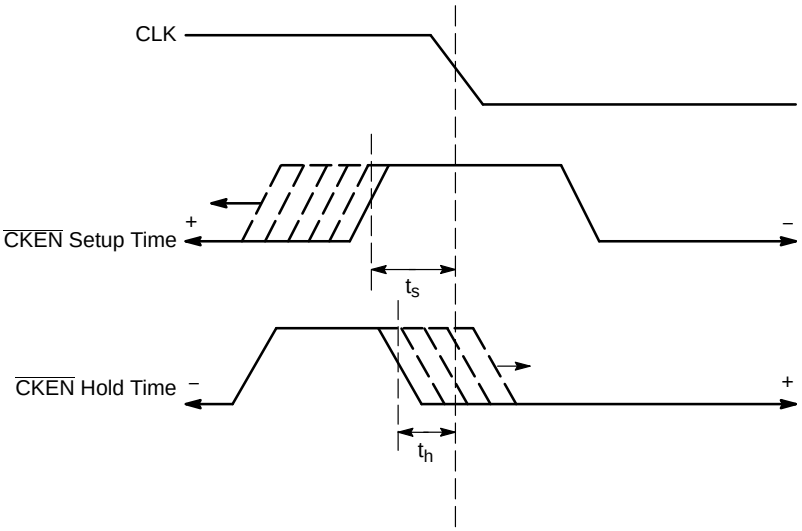


Figure 6. $\overline{CKEN}$ Setup and Hold Time

For CKSEL LOW operation, the data is latched on both the rising edge and the falling edge of the clock and the time from when the serial data is latched① to when the data is seen on the parallel output② is 6 clock cycles (see Figure 8).

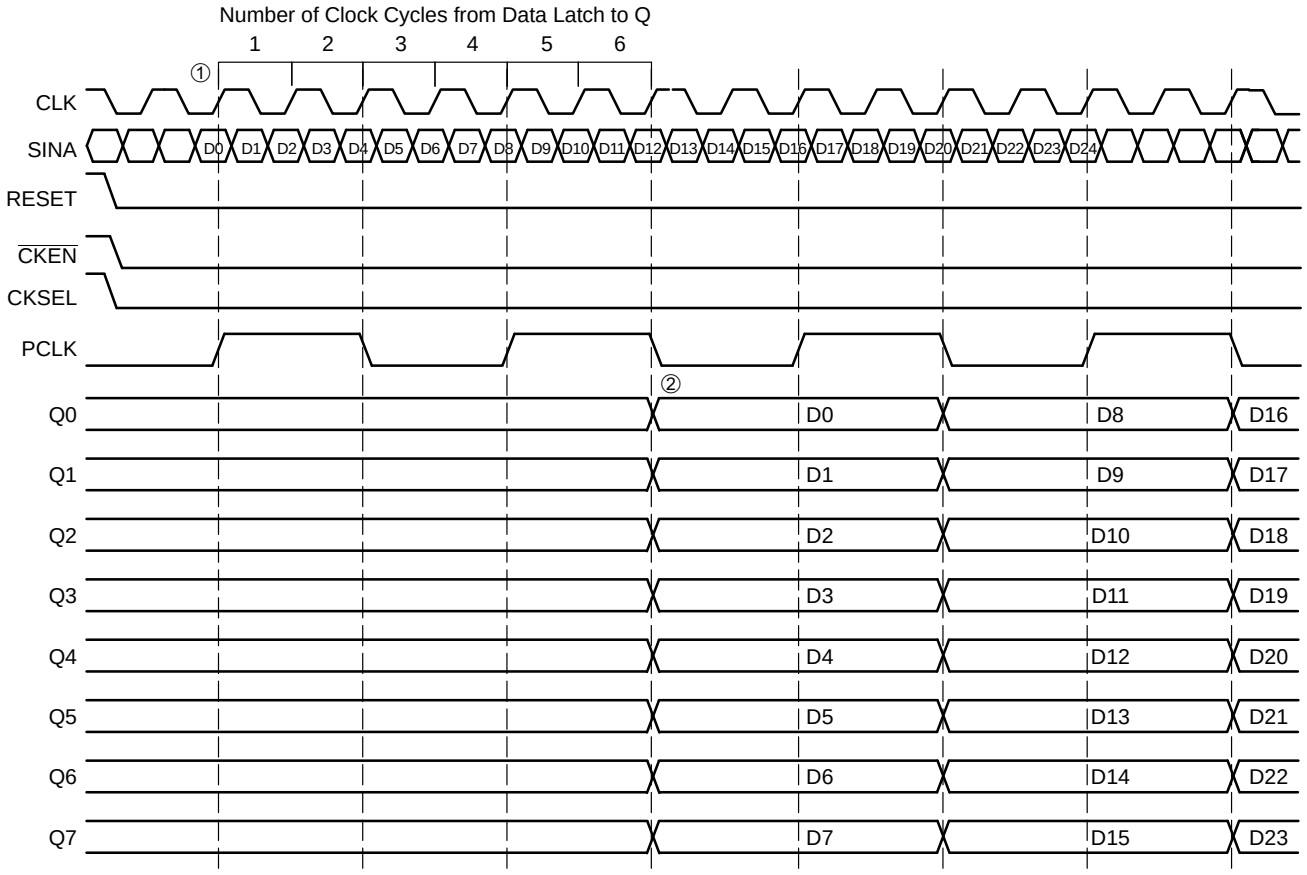


Figure 8. Timing Diagram A. 1:8 Serial to Parallel Conversion with CKSEL LOW

Similarly, for CKSEL HIGH operation, the data is latched only on the rising edge of the clock and the time from when the serial data is latched① to when the data is seen on the parallel output② is 12 clock cycles (see Figure 9).

Figure 9. Timing Diagram A. 1:8 Serial to Parallel Conversion with CKSEL HIGH

To allow the user to synchronize the output byte data correctly, the start bit for conversion can be moved using the SYNC input pin (pin 2). Asynchronously asserting the SYNC pin will force the internal clock to swallow a clock pulse, effectively shifting a bit from the Q_n to the Q_{n-1} output as shown in Figure 10 and Figure 11. For CKSEL LOW, a single pulse applied asynchronously for two consecutive clock cycles shifts the start bit for conversion from Q_n to Q_{n-1}. The bit is swallowed following the two clock cycle pulse width of SYNC① on the next triggering edge of clock② (either on the rising or the falling edge of the clock). Each additional shift requires an additional pulse to be applied to the SYNC pin. (See Figure 10)

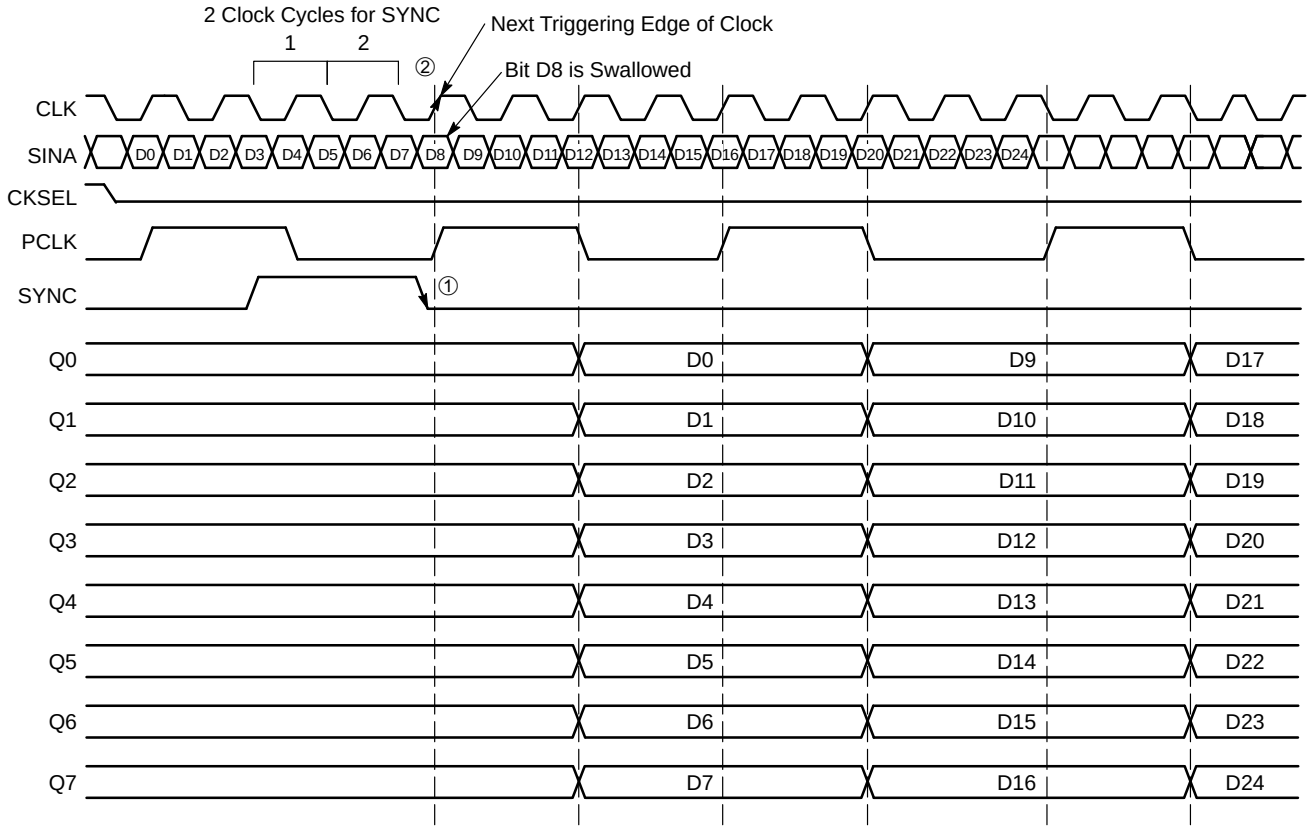


Figure 10. Timing Diagram A. 1:8 Serial to Parallel Conversion with SYNC Pulse at CKSEL LOW

For CKSEL HIGH, a single pulse applied asynchronously for three consecutive clock cycles shifts the start bit for conversion from Q_n to Q_{n-1}. The bit is swallowed following the three clock cycle pulse width of SYNC① on the next triggering edge of clock② (on the rising edge of the clock only). Each additional shift requires an additional pulse to be applied to the SYNC pin. (See Figure 11)

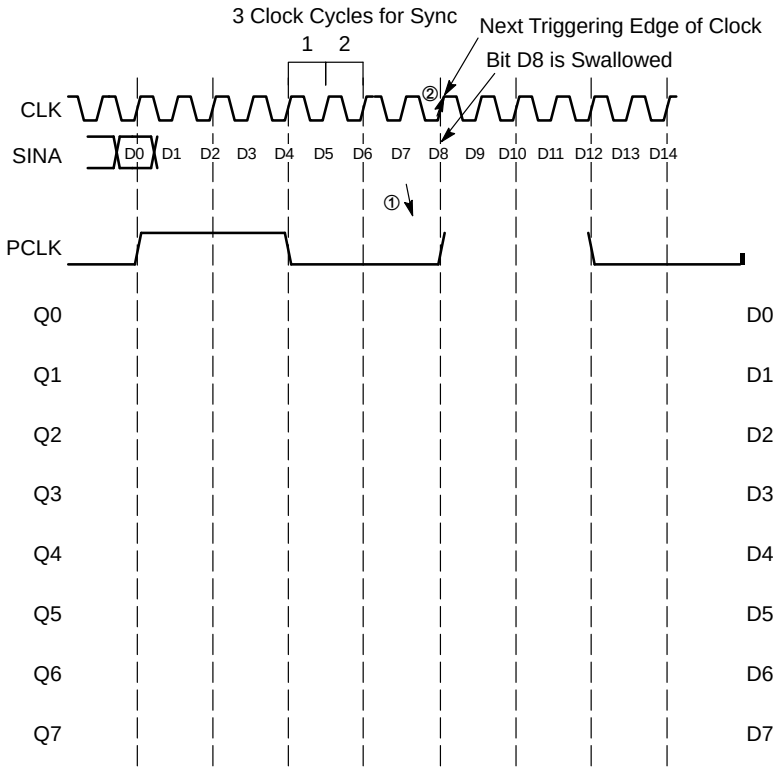


Figure 11. Timing Diagram A. 1:8 Serial to Parallel Conversion with SYNC Pulse at CKSEL HIGH

The synchronous $\overline{\text{CKEN}}$ (pin 3) applied with at least one clock cycle pulse length will disable the internal clock signal. The synchronous $\overline{\text{CKEN}}$ will suspend all of the device activities and prevent runt pulses from being generated. The rising edge of $\overline{\text{CKEN}}$ followed by the falling edge of CLK will suspend all activities. The first data bit will clock on the rising edge, since the falling edge of $\overline{\text{CKEN}}$ followed by the falling edge of the incoming clock triggers the enabling of the internal process. (See Figure 12)

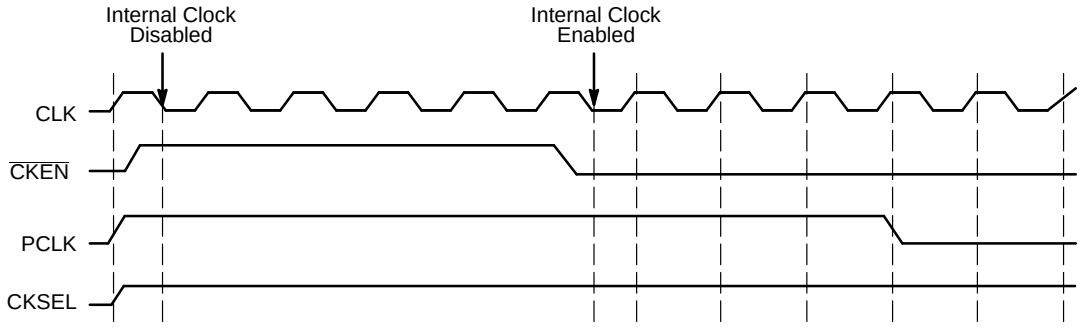


Figure 12. Timing Diagram with CKEN with CKSEL HIGH

The differential PCLK output (pins 22 and 23) is a word framer and can help the user to synchronize the parallel data outputs. During CKSEL LOW operation, the PCLK will provide a divide by 4−clock frequency, which frames the serial data in period of PCLK output. Likewise during CKSEL HIGH operation, the PCLK will provide a divide by 8−clock frequency.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single–ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a

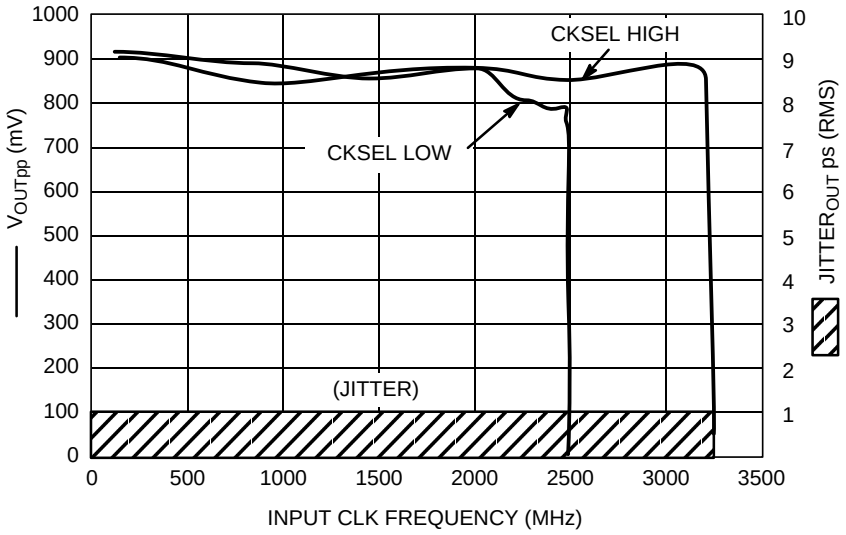


Figure 13. F_{max}/Jitter

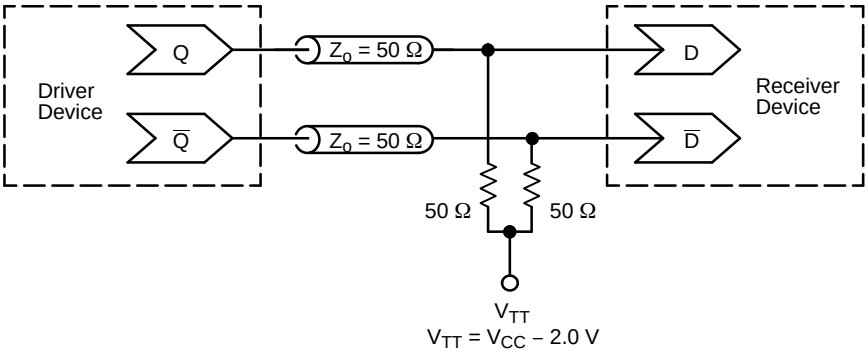


Figure 14. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

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