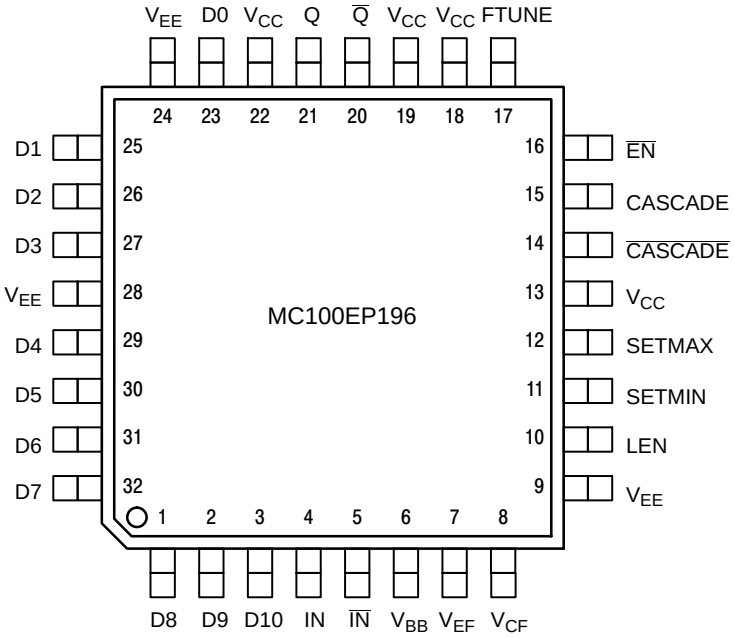

Figure 1. 32−Lead LQFP Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	State	Description
23, 25, 26, 27, 29, 30, 31, 32, 1, 2	D[0:9]	LVCMOS, LVTTL, ECL Input		Single−ended Parallel Data Inputs [0:9]. Internal 75 kΩ to
3	D[10]	LVCMOS, LVTTL, ECL Input	LOW	Single−ended CASCADE/$\overline{\text{CASCADE}}$ Control Input. Intern to V_{EE}. (Note 1)
4	IN	ECL Input		Noninverted Differential Input. Internal 75 kΩ to V
5	$\overline{\text{IN}}$	ECL Input	HIGH	Inverted Differential Input. Internal 75 kΩ to V_{EE}.
6	V_{BB}	−	−	ECL Reference Voltage Output
7	V_{EF}	−	−	Reference Voltage for ECL Mode Connection
8	V_{CF}	−	−	LVCMOS, ECL, OR LVTTL Input Mode Select
9, 28	V_{EE}	−	−	Negative Supply Voltage. All V_{EE} Pins must be Externally Connected to Power Supply to Guarantee Proper Operation. (Note 2)
13, 18, 19, 22	V_{CC}	−	−	Positive Supply Voltage. All V_{CC} Pins must be externally Connected to Power Supply to Guarantee Proper Operation. (Note 2)
10	LEN	ECL Input		Single−ended D pin [illegible] HOLD input. Internal 75 kΩ
11	SETMIN	ECL Input		Single− [illegible] inimum Delay Set Logic Input. Internal 75 k [illegible] te 1)
12	SETMAX	ECL Input	LOW	Single−ended Maximum Delay Set Logic Input. Internal 75 kΩ to V_{EE}. (Note 1)
14	$\overline{\text{CASCADE}}$	ECL Output		[illegible] minated with 50 Ω to $V_{TT} = V_{CC} - 2$ V.
15	CASCADE	ECL Output		Noninverted Differential Cascade Output [illegible] Typically Terminated with 50 Ω to [illegible] 2 V.
16	$\overline{\text{EN}}$	ECL Input		Single−ended Output Enable Pin. Internal 75 kΩ to V_{EE}.
17	FTUNE	Analog Input		[illegible] uning Input.
21	Q	ECL Output	−	

Table 2. CONTROL PIN

Pin	State	Function
EN	LOW (Note 3)	Input Signal is Propagated to the Output
	HIGH	Output Holds Logic Low State
LEN	LOW (Note 3)	Transparent or LOAD mode for real time delay values present on D[0:10].
	HIGH	LOCK and HOLD mode for delay values on D[0:10]; further changes on D[0:10] are not recognized and do not affect delay.
SETMIN	LOW (Note 3)	Output Delay set by D[0:10]
	HIGH	Set Minimum Output Delay
SETMAX	LOW (Note 3)	Output Delay set by D[0:10]
	HIGH	Set Maximum Output Delay
D10	LOW	CASCADE Output LOW, $\overline{\text{CASCADE}}$ Output HIGH
	HIGH	$\overline{\text{CASCADE}}$ Output LOW, CASCADE Output High

3. Internal pulldown resistor will provide a logic LOW if pin is left unconnected.

Table 3. CONTROL D[0:10] INTERFACE

Pin	State	Function
V_{CF}	V_{EF} Pin (Note 4)	ECL Mode
V_{CF}	No Connect	LVCMOS Mode
V_{CF}	1.5 V ± 100 mV	LVTTL Mode (Note 5)

4. Short V_{CF} (pin 8) and V_{EF} (pin 7).
5. When Operating in LVTTL Mode, the reference voltage can be provided by connecting an external resistor, R_{CF} (suggested resistor value is 2.2 kΩ ±5%), between V_{CF} and V_{EE} pins.

Table 4. DATA INPUT ALLOWED OPERATING VOLTAGE MODE TABLE

POWER SUPPLY	CONTROL DATA SELECT INPUTS PINS (D [0:10])			
	LVCMOS	LVTTL	LVPECL	LVNECL
PECL Mode Operating Range	YES	YES	YES	N/A
NECL Mode Operating Range	N/A	N/A		

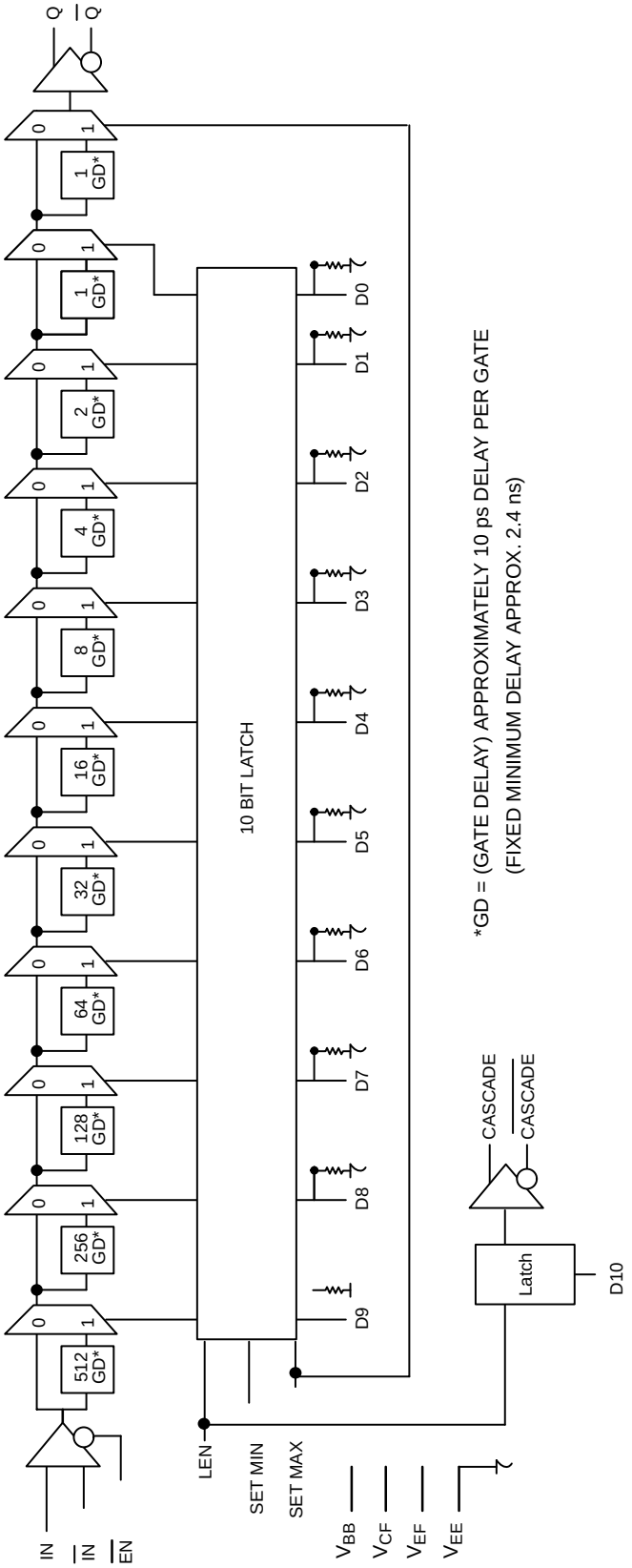

Figure 2. Logic Diagram

Table 5. THEORETICAL DELTA DELAY VALUES

D(9:0) Value	SETMIN	SETMAX	Programmable Delay*
XXXXXXXXXX	H	L	0 ps
0000000000	L	L	0 ps
0000000001	L	L	10 ps
0000000010	L	L	20 ps
0000000011	L	L	30 ps
0000000100	L	L	40 ps
0000000101	L	L	50 ps
0000000110	L	L	60 ps
0000000111	L	L	70 ps
0000001000	L	L	80 ps
0000010000	L	L	160 ps
0000100000	L	L	320 ps
0001000000	L	L	640 ps
0010000000	L	L	1280 ps
0100000000	L	L	2560 ps
1000000000	L	L	5120 ps
1111111111	L	L	10230 ps
XXXXXXXXXX	L	H	10240 ps

*Fixed minimum delay not included.

Table 6. TYPICAL FTUNE DELAY PIN

Input Range	Output Range
V_{CC}–V_{EE} (V)	0 − 60 (ps)

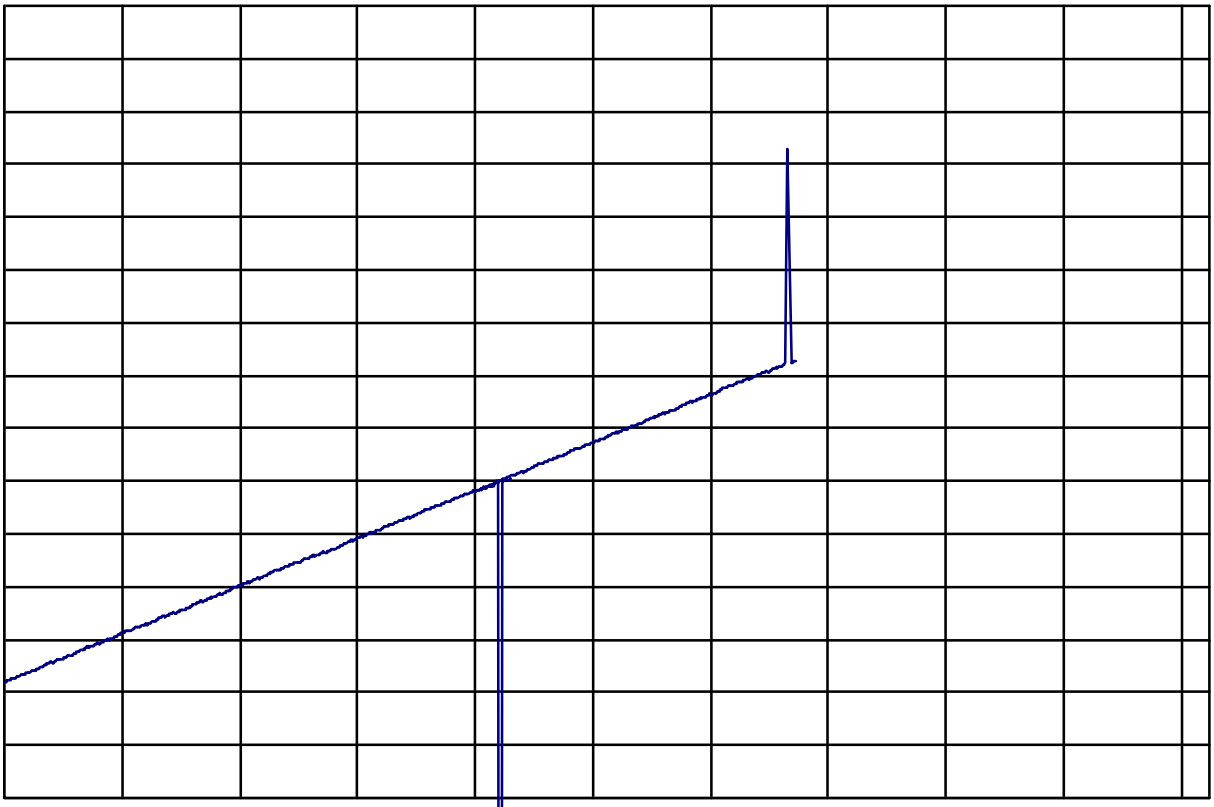

Table 8. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		−6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 −6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	LQFP−32 LQFP−32	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	LQFP−32	12 to 17	°C/W
T_{sol}	Wave Solder Pb−Free			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 9. DC CHARACTERISTICS, PECL V

Table 10. DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = −3.3 V (Note 5)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	100	125	160	110	130	170	110	135	175	mA
V_{OH}	Output HIGH Voltage (Note 6)	−1145	−1000	−895	−1145	−1000	−895	−1145	−1000	−895	mV
V_{OL}	Output LOW Voltage (Note 6)	−1995	−1780	−1695	−1995	−1800	−1695	−1995	−1815	−1695	mV
V_{IH}	Input HIGH Voltage (Single−Ended) LVNECL	−1225		−880	−1225		−880	−1225		−880	mV
V_{IL}	Input LOW Voltage (Single−Ended) LVNECL	−1995		−1625	−1995		−1625	−1995		−1625	mV
V_{BB}											

Table 11. AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = −3.0 V to −3.6 V or V_{CC} = 3.0 V to 3.6 V; V_{EE} = 0 V (Note 8)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Frequency		1.2			1.2			1.2		GHz
t_{PLH} t_{PHL}	Propagation Delay										ps
	IN to Q; D(0−9) = 0	1810	2210	2610	1960	2360	2760	2180	2580	2980	
	IN to Q; D(0−9) = 1023	9500	11496	13500	10000	12258	14000	10955	13454	15955	
	$\overline{EN}$ to Q; D(0−9) = 0	1780	2277	2780	1930	2430	2930	2150	2650	3150	
	D10 to CASCADE	350	450	550	380	477	580	420	520	620	
t_{RANGE}	Programmable Range {D(0−9) = HI} − {D(0−9) = LO}	8600	9285	10000	9200	9897	10700	9900	10875	12000	ps
Δt	Step Delay (Note 9)										
	D0 High										
	D1 High										
	D2 High										
	D3 High										
	D4 High	90									
	D5 High	245									
	D6 High	530									
	D7 High	1060									
	D8 High										
	D9 High										

CASCADING MULTIPLE EP196S

To increase the programmable range of the EP196, internal cascade circuitry has been included. This circuitry allows for the cascading of multiple EP196s without the need for any external gating. Furthermore, this capability requires only one more address line per added E196. Obviously, cascading multiple programmable delay chips will result in a larger programmable range; however, this increase is at the expense of a longer minimum delay.

Figure 6 illustrates the interconnect scheme for cascading two EP196s. As can be seen, this scheme can easily be expanded for larger EP196 chains. The D10 input of the EP196 is the cascade control pin and when assert HIGH switches output pin CASCADE to HIGH and pin $\overline{\text{CASCADE}}$ to LOW. With the interconnect scheme of Figure 6 when D10 is asserted, it signals the need for a larger programmable range than is achievable with a single device. The A11 address can be added to generate a cascade output for the next EP196. For a 2−device configuration, A11 is not required.

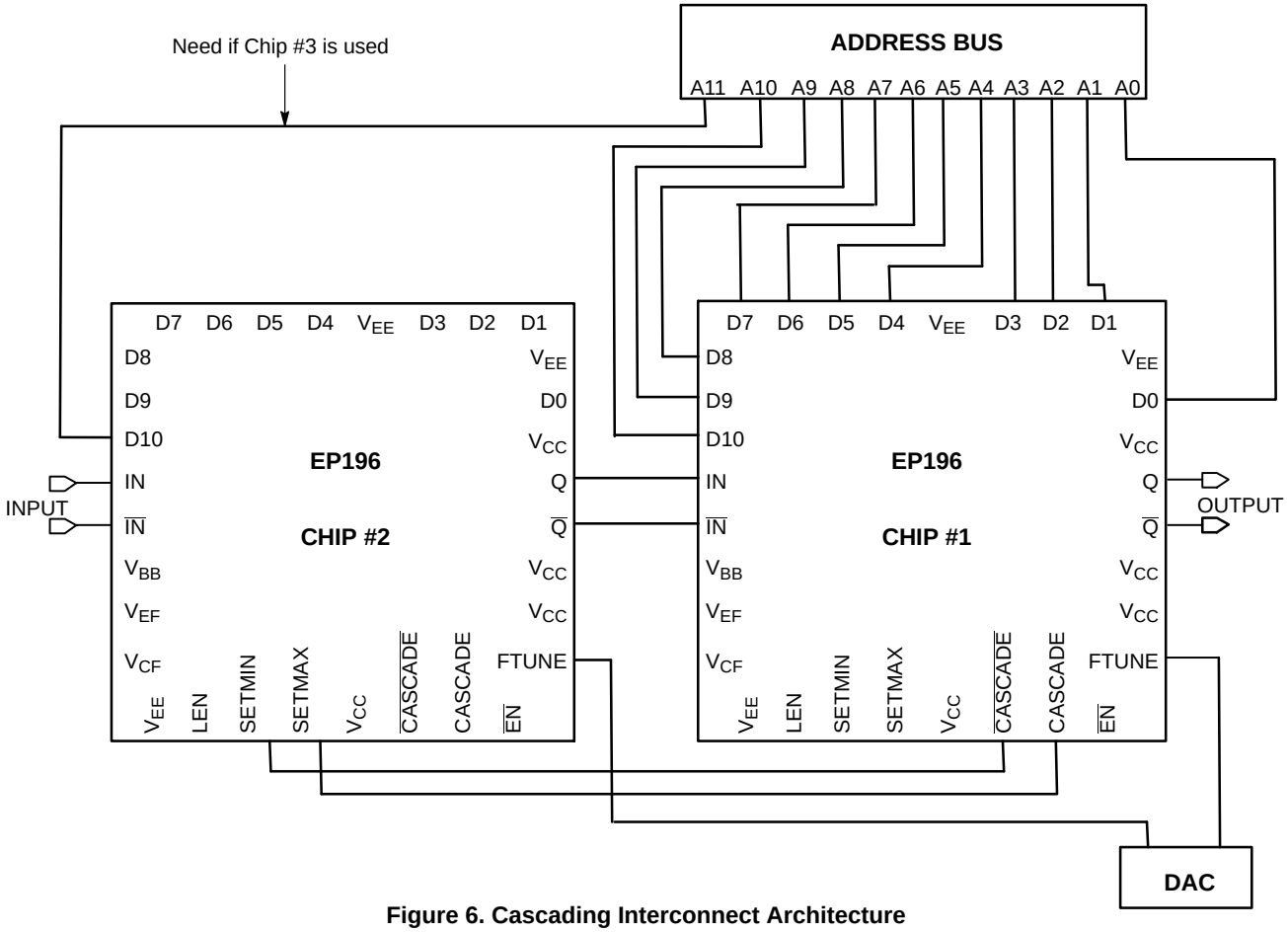

Figure 6. Cascading Interconnect Architecture

An expansion of the latch section of the block diagram is pictured in Figure 7. Use of this diagram will simplify the explanation of how the SETMIN and SETMAX circuitry works in cascade. When D10 of chip #1 in Figure 5 is LOW, this device's cascade output will also be LOW while the $\overline{\text{CASCADE}}$ output will be HIGH. In this condition, the SETMIN pin of chip #2 will be asserted HIGH and thus all of the latches of chip #2 will be reset and the device will be set at its minimum delay.

Chip #1, on the other hand, will have both SETMIN and SETMAX deasserted so that its delay will be controlled entirely by the address bus A0−A9. If the delay needed is greater than can be achieved with 1023 gate delays (1111111111 on the A0−A9 address bus), D10 will be asserted to signal the need to cascade the delay to the next EP196 device. When D10 is asserted, the SETMIN pin of chip #2 will be deasserted and the SETMAX pin asserted, resulting in the device delay to be the maximum delay. Table 12 shows the delay time of two EP196 chips in cascade.

To expand this cascading scheme to more devices, one simply needs to connect the D10 pin from the next chip to the address bus and CASCADE outputs to the next chip in the same manner as pictured in Figure 6. The only addition to the logic is the increase of one line to the address bus for cascade control of the second programmable delay chip.

Furthermore, to fully utilize EP196, the FTUNE pin can be used for additional delay and for finer resolution than 10 ps. As shown in Figure 5, an analog voltage input from DAC can adjust the FTUNE pin with an extra 60 ps of delay for each chip.

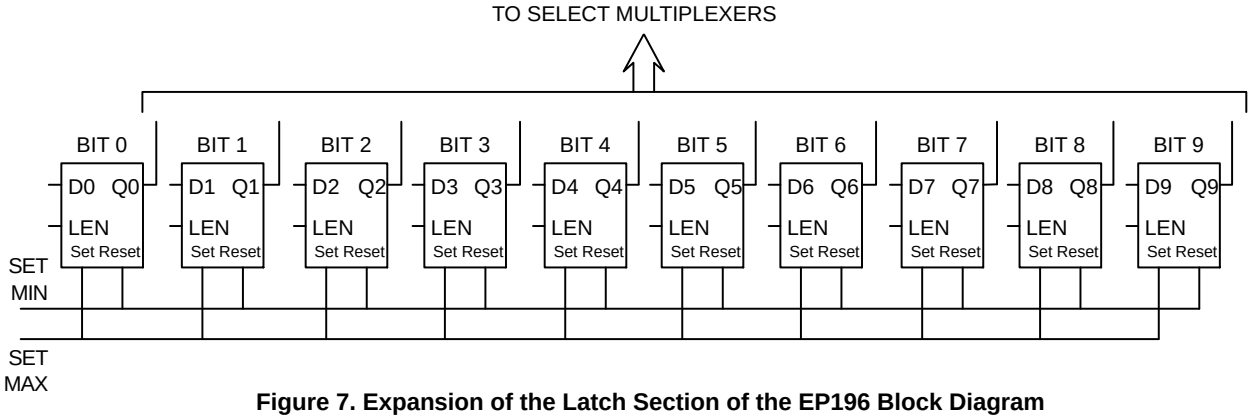

Figure 7. Expansion of the Latch Section of the EP196 Block Diagram

Table 12. CASCADED DELAY VALUE OF TWO EP196S

VARIABLE INPUT TO CHIP #1 AND *SETMIN* FOR CHIP #2												
INPUT FOR CHIP #1												Total
D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Delay Value	Delay Value
0	0	0	0	0	0	0	0	0	0	0	0 ps	4400 ps
0	0	0	0	0	0	0	0	0	0	1	10 ps	4410 ps
0	0	0	0	0	0	0	0	0	1	0	20 ps	4420 ps
0	0	0	0	0	0	0	0	0	1	1	30 ps	4430 ps
0	0	0	0	0	0	0	0	1	0	0	40 ps	4440 ps
0	0	0	0	0	0	0	0	1	0	1	50 ps	4450 ps
0	0	0	0	0	0	0	0	1	1	0	60 ps	4460 ps
0	0	0	0	0	0	0	0	1	1	1	70 ps	4470 ps
0	0	0	0	0	0	0	1	0	0	0	80 ps	4480 ps
0	0	0	0	0	0	1	0	0	0	0	160 ps	4560 ps
0	0	0	0	0	1	0	0	0	0	0	320 ps	4720 ps
0	0	0	0	1	0	0	0	0	0	0	640 ps	5040 ps
0	0	0	1	0	0	0	0	0	0	0	1280 ps	5680 ps
0	0	1	0	0	0	0						

MULTI−CHANNEL DESKEWING

The most practical application for EP196 is in multiple channel delay matching. Slight differences in impedance and cable length can create large timing skews within a high−speed system. To deskew multiple signal channels, each channel can be sent through each EP196 as shown in Figure 8. One signal channel can be used as reference and the other EP196s can be used to adjust the delay to eliminate the timing skews. Nearly any high−speed system can be fine tuned (as small as 10 ps) to reduce the skew to extremely tight tolerances using the available FTUNE pin.

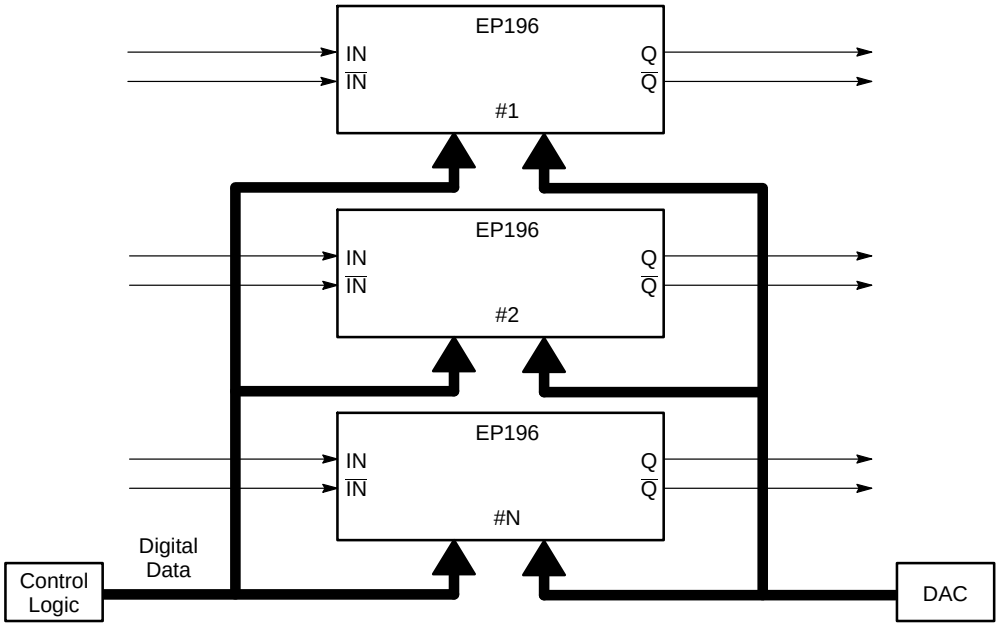

Figure 8. Multiple Channel Deskewing Diagram

MC100EP196