3.3 V ECL Programmable Delay Chip

MC100EP195B

Descriptions

The MC100EP195B is a Programmable Delay Chip (PDC) designed primarily for clock deskewing and timing adjustment. It provides variable delay of a differential NECL/PECL input transition.

The delay section consists of a programmable matrix of gates and multiplexers as shown in the logic diagram, Figure 2. The delay increment of the EP195B has a digitally selectable resolution of about 10 ps and a net range of up to 10.2 ns. The required delay is selected by the 10 data select inputs D[9:0] values and controlled by the LEN (pin 10). A LOW level on LEN allows a transparent LOAD mode of real time delay values by D[9:0]. A LOW to HIGH transition on LEN will LOCK and HOLD current values present against any subsequent changes in D[10:0]. The approximate delay values for varying tap numbers correlating to D0 (LSB) through D9 (MSB) are shown in Table 6 and Figure 3.

The IN/$\overline{\text{IN}}$ inputs can accept LVPECL (SE of Diff), or LVDS level signals. Because the EP195B is designed using a chain of multiplexers it has a fixed minimum delay of 2.2 ns. An additional pin D10 is provided for controlling Pins 14 and 15, CASCADE and $\overline{\text{CASCADE}}$, also latched by LEN, in cascading multiple PDCs for increased programmable range. The cascade logic allows full control of multiple PDCs. Switching devices from all “1” states on D[0:9] with SETMAX LOW to all “0” states on D[0:9] with SETMAX HIGH will increase the delay equivalent to “D0”, the minimum increment.

Select input pins D[10:0] may be threshold controlled by combinations of interconnects between V_{EF} (pin 7) and V_{CF} (pin 8) for LVCMOS, ECL, or LVTTL level signals. For LVCMOS input levels, leave V_{CF} and V_{EF} open. For ECL operation, short V_{CF} and V_{EF}

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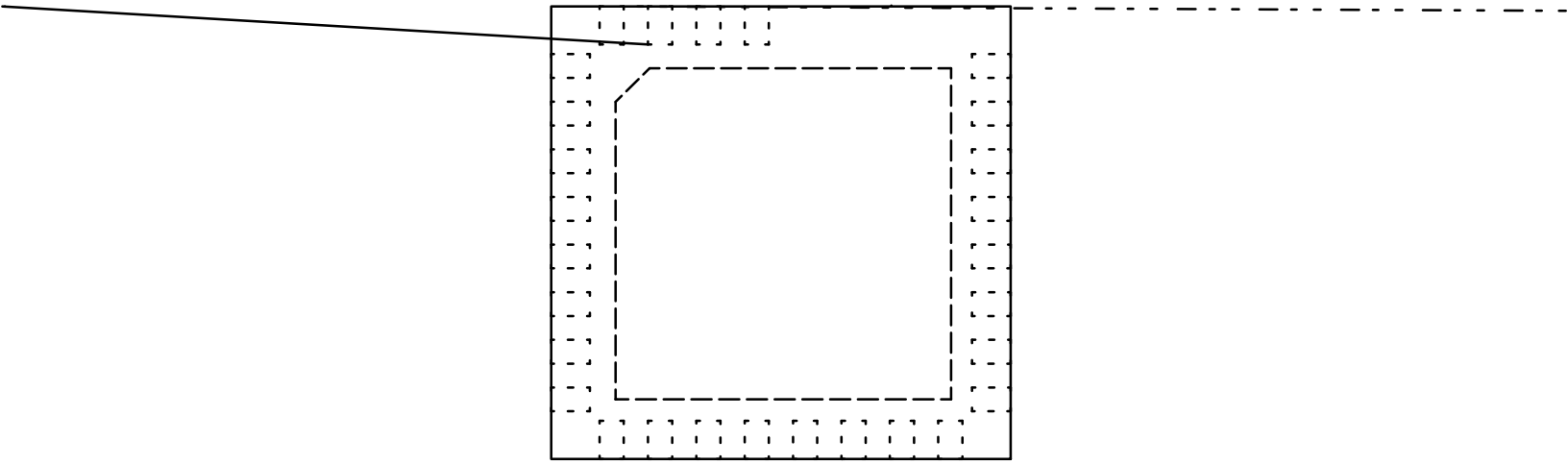


Table 1. PIN DESCRIPTION

Pin	Name	I/O	Default State	Description
23, 25, 26, 27, 29, 30, 31, 32, 1, 2	D[0:9]	LVCMOS, LVTTL, ECL Input	Low	Single−Ended Parallel Data Inputs [0:9]. Internal 75 kΩ to V_{EE}. (Note 1)
3	D[10]	LVCMOS, LVTTL, ECL Input	Low	Single−Ended CASCADE/$\overline{\text{CASCADE}}$ Control Input. Internal 75 kΩ to V_{EE}. (Note 1)
4	IN	LVPECL, LVDS	Low	Noninverted Differential Input. Internal 75 kΩ to V_{EE}.
5	$\overline{\text{IN}}$	LVPECL, LVDS	High	Inverted Differential Input. Internal 75 kΩ to V_{EE} and 36.5 kΩ to V_{CC}.
6	V_{BB}	−	−	ECL Reference Voltage Output
7	V_{EF}	−	−	Reference Voltage for ECL Mode Connection
8	V_{CF}	−	−	LVCMOS, ECL, OR LVTTL Input Mode Select
9, 24, 28	V_{EE}	−	−	Negative Supply Voltage. All V_{EE} Pins must be Externally Connected to Power Supply to Guarantee Proper Operation. (Note 2)
13, 18, 19, 22	V_{CC}	−	−	Positive Supply Voltage. All V_{CC} Pins must be externally Connected to Power Supply to Guarantee Proper Operation. (Note 2)
10				

Table 2. CONTROL PIN

Pin	State	Function
EN	LOW (Note 3)	Input Signal is Propagated to the Output
	HIGH	Output Holds Logic Low State
LEN	LOW (Note 3)	Transparent or LOAD mode for real time delay values present on D[0:10].
	HIGH	LOCK and HOLD mode for delay values on D[0:10]; further changes on D[0:10] are not recognized and do not affect delay.
SETMIN	LOW (Note 3)	Output Delay set by D[0:10]
	HIGH	Set Minimum Output Delay
SETMAX	LOW (Note 3)	Output Delay set by D[0:10]
	HIGH	Set Maximum Output Delay
D10	LOW (Note 3)	CASCADE Output LOW, $\overline{\text{CASCADE}}$ Output HIGH
	HIGH	$\overline{\text{CASCADE}}$ Output LOW, CASCADE Output HIGH

3. Internal pulldown resistor will provide a logic LOW if pin is left unconnected.

Table 3. CONTROL D[0:10] INTERFACE

V_{CF}	V_{EF} Pin (Note 4)	ECL Mode
V_{CF}	No Connect	LVCMOS Mode
V_{CF}	1.5 V ±100 mV	LVTTL Mode (Note 5)

4. Short V_{CF} (pin 8) and V_{EF} (pin 7).

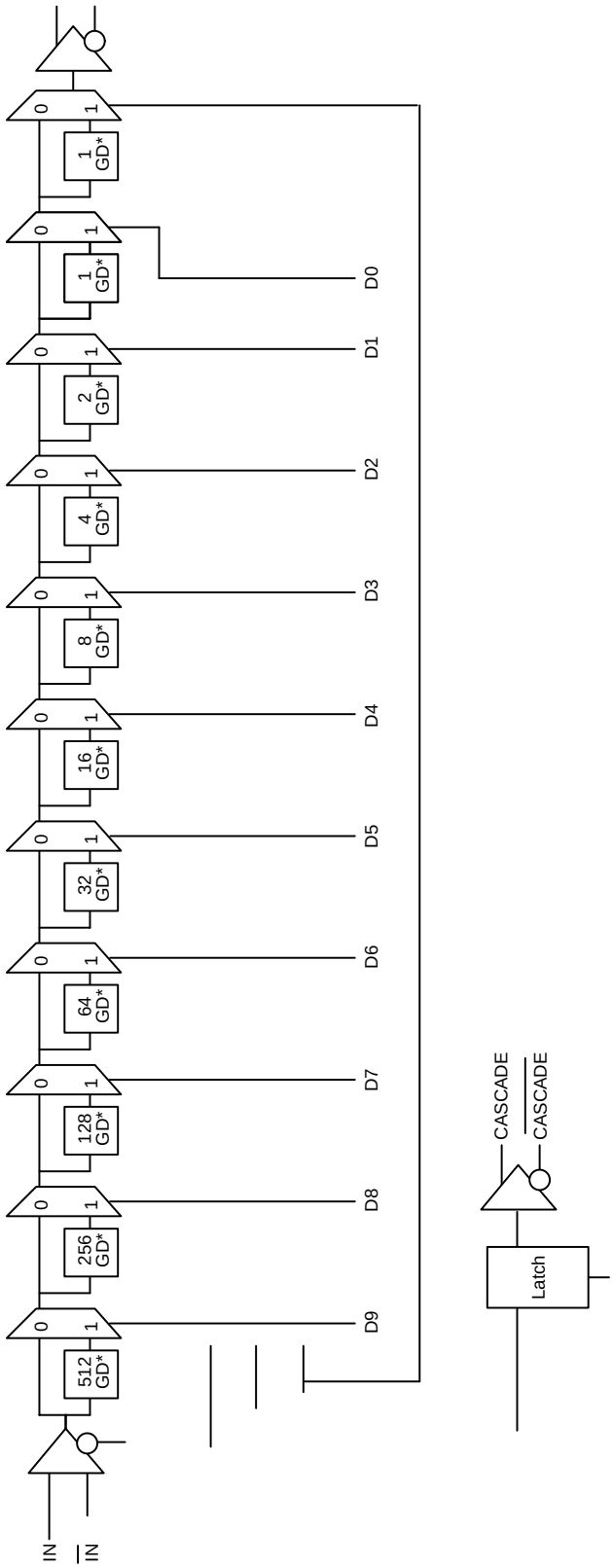

0
1
1
GD*
D0
2
4
8
16
32
64
128
256
512
D1
D2
D3
D4
D5
D6
D7
D8
D9
IN
IN
CASCADE
CASCADE
Latch

Table 6. THEORETICAL DELAY VALUES

D(9:0) Value	SETMIN	SETMAX	Programmable Delay*
XXXXXXXXXX	H	L	0 ps
0000000000	L	L	0 ps
0000000001	L	L	10 ps
0000000010	L	L	20 ps
0000000011	L	L	30 ps
0000000100	L	L	40 ps
0000000101	L	L	50 ps
0000000110	L	L	60 ps
0000000111	L	L	70 ps
0000001000	L	L	80 ps
0000010000	L	L	160 ps
0000100000			

Table 7. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	Negative Mode Power Supply	V_{CC} = 0 V		−6	V
V_I	Positive Mode Input Voltage Negative Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 −6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			±0.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	QFN−32 QFN−32	31 27	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	2S2P Standard Board	QFN−32	12	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	LQFP−32 LQFP−32	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	2S2P Standard Board	LQFP−32	12 to 17	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 260°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 8. 100EP DC CHARACTERISTICS, PECL (V_{CC} = 3.3 V, V_{EE} = 0 V) (Note 7)

		−40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Negative Power Supply Current	90	115	170	100	140	170	100	145	170	mA
V_{OH}	Output HIGH Voltage (Note 8)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 8)	1305	1480	1605	1305	1480	1605	1305	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single−Ended) LVPECL CMOS TTL	 2075 2000 2000		 2420 3300 3300	 2075 2000 2000		 2420 3300 3300	 2075 2000 2000		 2420 3300 3300	mV
V_{IL}	Input LOW Voltage (Single−Ended) LVPECL CMOS TTL	 1305 0 0		 1675 800 800	 1305 0 0		 1675 800 800	 1305 0 0		 1675 800 800	mV
V_{BB}	ECL Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{CF}											

Table 10. AC CHARACTERISTICS (V_{CC} = 0 V; V_{EE} = −3.0 V to −3.6 V or V_{CC} = 3.0 V to 3.6 V; V_{EE} = 0 V) (Note 14) (continued)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**

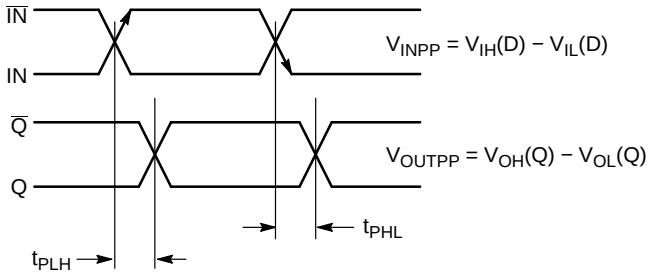


Figure 4. AC Reference Measurement

Cascading Multiple EP195Bs

To increase the programmable range of the EP195B, internal cascade circuitry has been included. This circuitry allows for the cascading of multiple EP195Bs without the need for any external gating. Furthermore, this capability requires only one more address line per added E195B. Obviously, cascading multiple programmable delay chips will result in a larger programmable range: however, this increase is at the expense of a longer minimum delay.

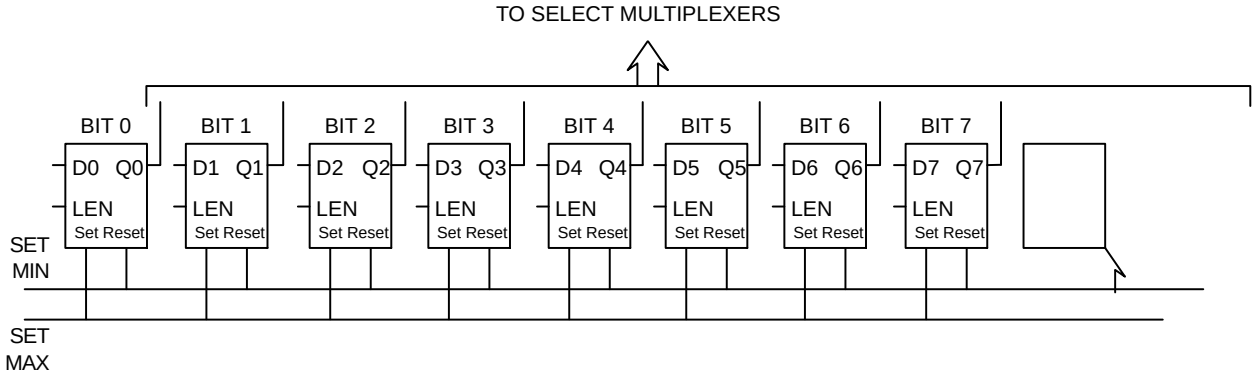
Figure 5 illustrates the interconnect scheme for cascading two EP195Bs. As can be seen, this scheme can easily be expanded for larger EP195B chains. The D10 input of the EP195B is the CASCADE control pin. With the interconnect scheme of Figure 5 when D10 is asserted, it signals the need for a larger programmable range than is achievable with a single device and switches output pin CASCADE HIGH and pin $\overline{\text{CASCADE}}$ LOW. The A11 address can be added to generate a cascade output for the next EP195B. For a 2−device configuration, A11 is not required.

V

V42cm 0 0 m12.076 -24.151 lS 1 0 0 1 0 24.151 cm 0 0 m12.076 -24.151 lS 1 0 0 1 60.265 -24.151 cm 0 0 m1614-

asserted to signal the need to cascade the delay to the next EP195B device. When D10 is asserted, the SET MIN pin of chip #2 will be deasserted and SET MAX pin asserted resulting in the device delay to be the maximum delay. Table 11 shows the delay time of two EP195B chips in cascade.

To expand this cascading scheme to more devices, one simply needs to connect the D10 pin from the next chip to the address bus and CASCADE outputs to the next chip in the same manner as pictured in Figure 5. The only addition to the logic is the increase of one line to the address bus for cascade control of the second programmable delay chip.



Multi−Channel Deskewing

The most practical application for EP195B is in multiple channel delay matching. Slight differences in impedance and cable length can create large timing skews within a high−speed system. To deskew multiple signal channels, each channel can be sent through each EP195B as shown in Figure 7. One signal channel can be used as reference and the other EP195Bs can be used to adjust the delay to eliminate the timing skews. Nearly any high−speed system can be fine−tuned (as small as 10 ps) to reduce the skew to extremely tight tolerances.

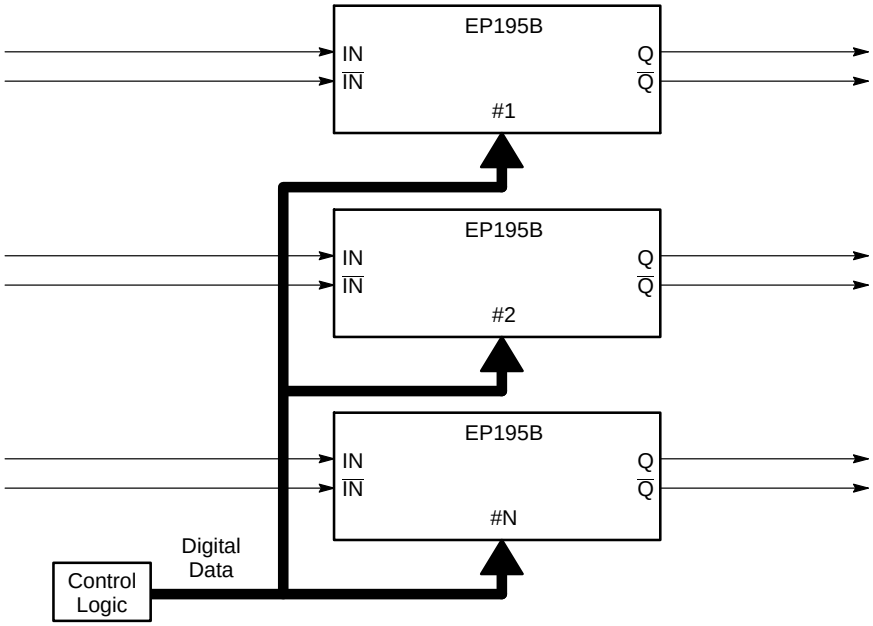


Figure 7. Multiple Channel Deskewing Diagram

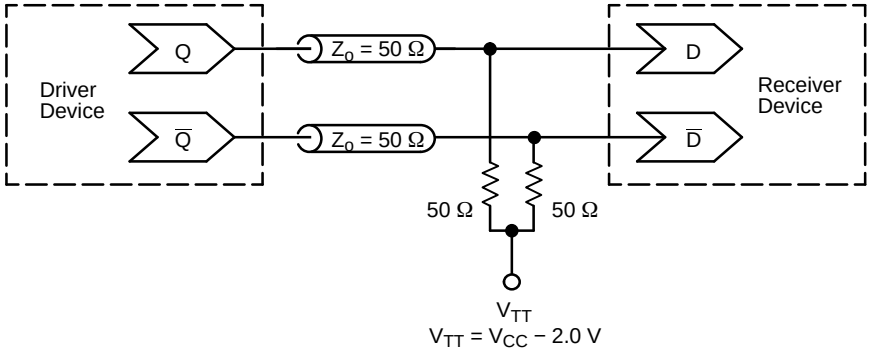


Figure 9. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1405/D − ECL Clock Distribution Techniques

AN1406/D − Designing with PECL (ECL at +5.0 V)

AN1503/D − ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D − Metastability and the ECLinPS Family

AN1568/D − Interfacing Between LVDS and ECL

AN1642/D − The ECL Translator Guide

AND8001/D − Odd Number Counters Design

AND8002/D − Marking and Date Codes

AND8020/D − Termination of ECL Logic Devices

AND8066/D − Interfacing with ECLinPS

AND8090/D − AC Characteristics of ECL Devices

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

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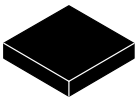
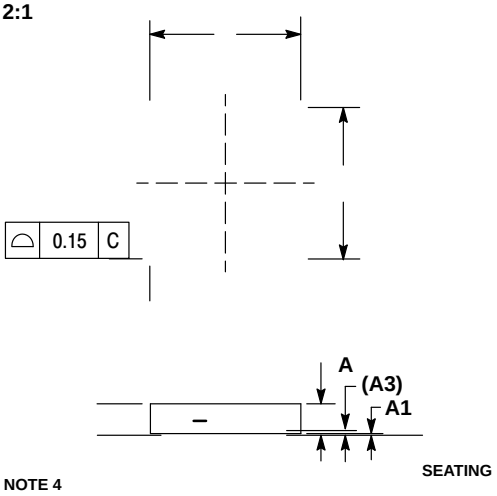
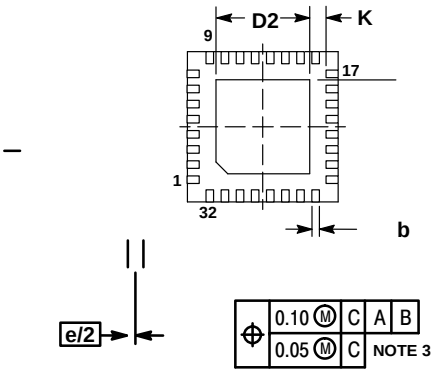


SCALE 2:1

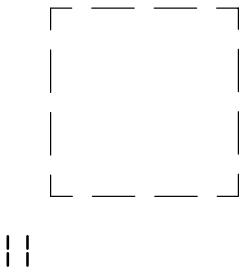


	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15



XXXXXXXX
XXXXXXXX
AWLYYWW▪
▪Free indicator, “G” or

RECOMMENDED



PITCH

DIMENSION: MILLIMETERS

DOCUMENT NUMBER:	98AON20032D	