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# LM555

## Single Timer

### Features

- High-Current Drive Capability: 200 mA
- Adjustable Duty Cycle
- Temperature Stability of 0.005%/°C
- Timing From  $\mu\text{s}$  to Hours
- Turn off Time Less Than 2  $\mu\text{s}$

### Applications

- Precision Timing
- Pulse Generation
- Delay Generation
- Sequential Timing

### Description

The LM555 is a highly stable controller capable of producing accurate timing pulses. With a monostable operation, the delay is controlled by one external resistor and one capacitor. With astable operation, the frequency and duty cycle are accurately controlled by two external resistors and one capacitor.

8-DIP



8-SOIC



### Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
LM555CN	0 ~ +70°C	LM555CN	DIP 8L	Rail
LM555CM		LM555CM	SOIC 8L	Rail
LM555CMX		LM555CM	SOIC 8L	Tape & Reel

## Block Diagram

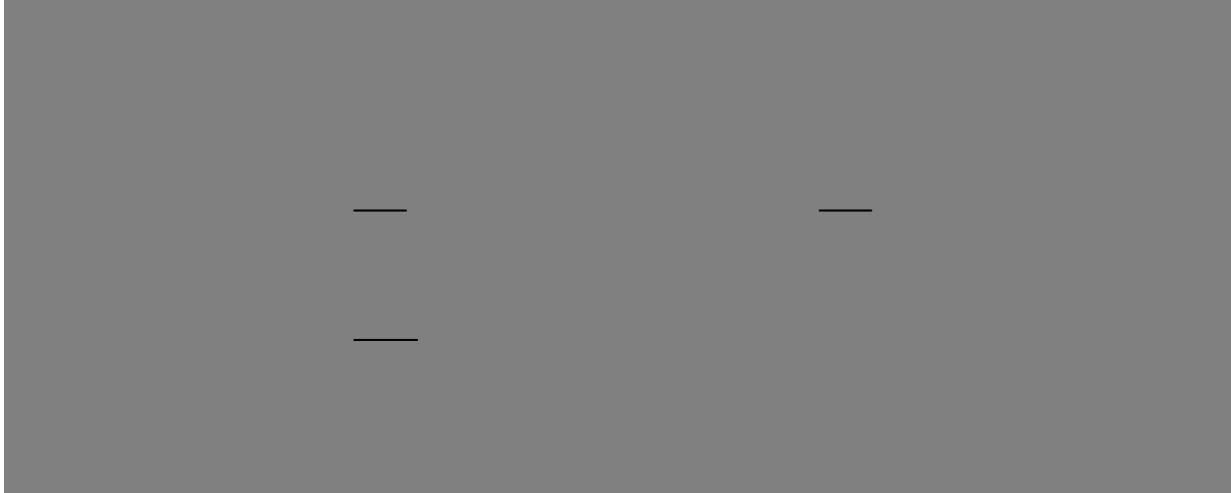


Figure 1. Block Diagram

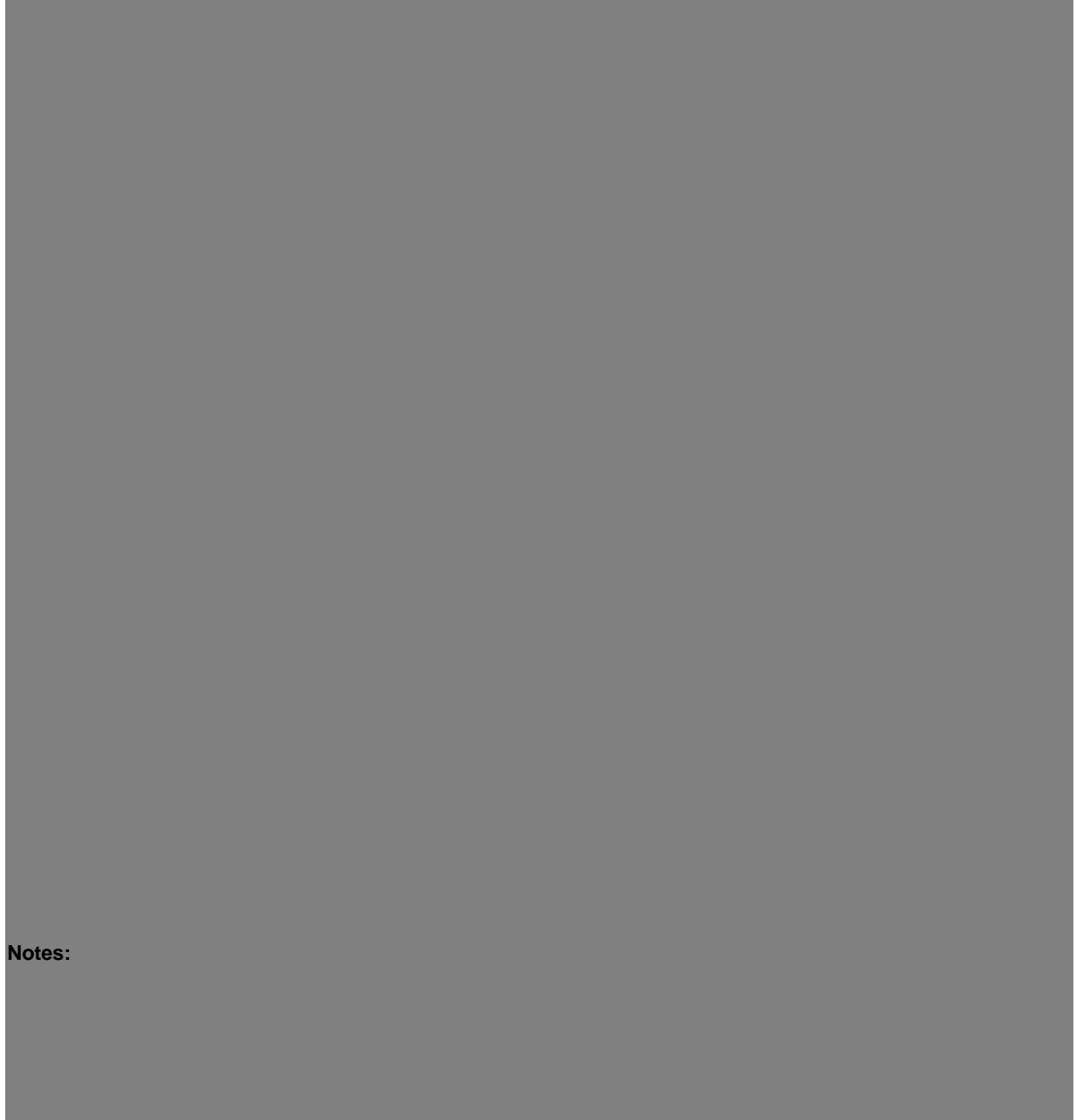
## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

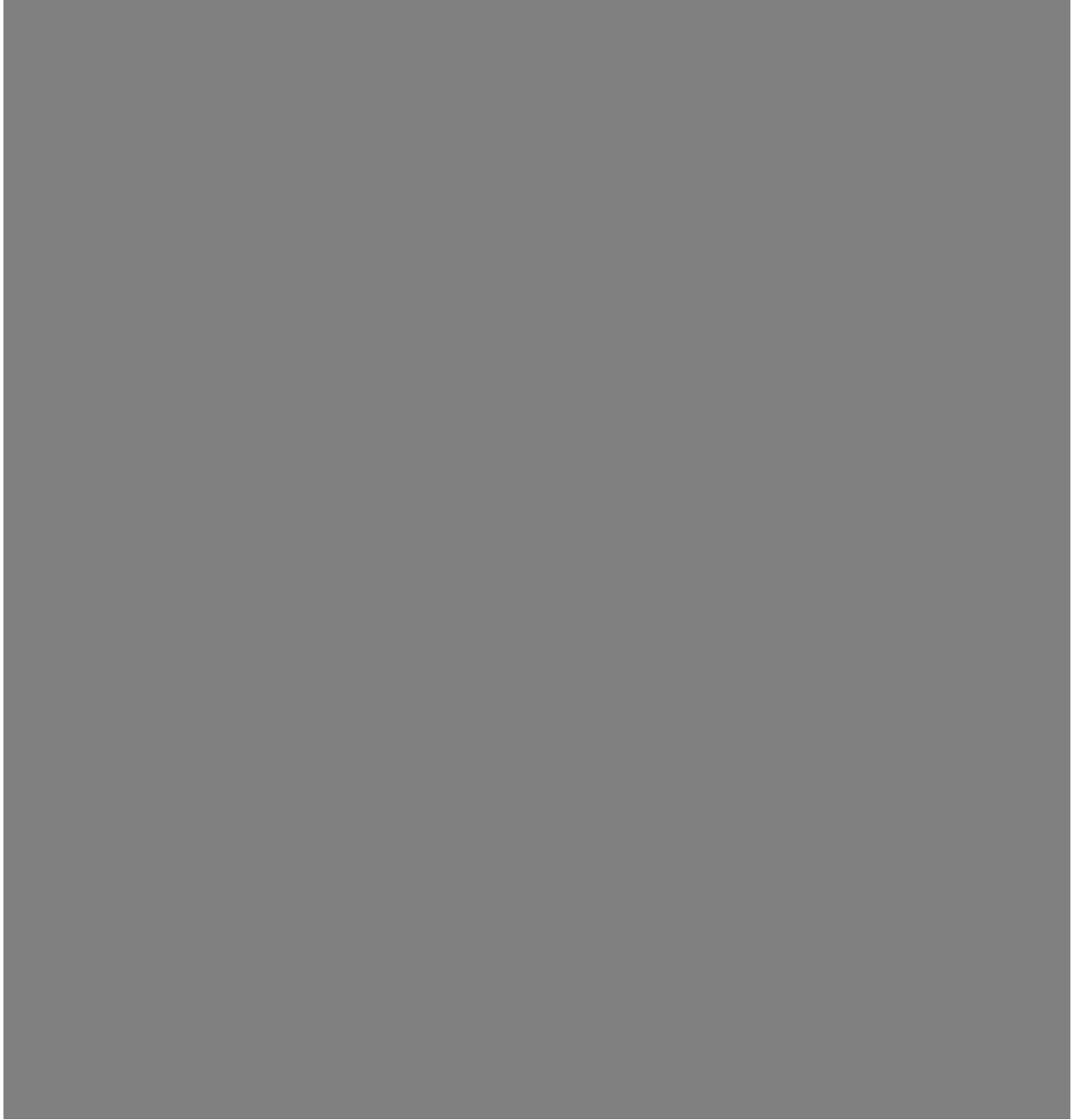
Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	16	V
$T_{LEAD}$	Lead Temperature (Soldering 10s)	300	$^\circ\text{C}$
$P_D$	Power Dissipation	600	mW
$T_{OPR}$	Operating Temperature Range	0 ~ +70	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-65 ~ +150	$^\circ\text{C}$

## Electrical Characteristics

Values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5 \sim 15\text{ V}$  unless otherwise specified.



Notes:



## 1. Monostable Operation

Figure 2 illustrates a monostable circuit. In this mode, the timer generates a fixed pulse whenever the trigger voltage falls below  $V_{CC}/3$ . When the trigger pulse voltage applied to the #2 pin falls below  $V_{CC}/3$  while the timer output is low, the timer's internal flip-flop turns the discharging transistor off and causes the timer output to become high by charging the external capacitor C1 and setting the flip-flop output at the same time.

The voltage across the external capacitor C1,  $V_{C1}$  increases exponentially with the time constant  $t = R_A * C$  and reaches  $2 V_{CC}/3$  at  $t_D = 1.1 R_A * C$ . Hence, capacitor C1 is charged through resistor  $R_A$ . The greater the time constant  $R_A C$ , the longer it takes for the  $V_{C1}$  to reach  $2 V_{CC}/3$ . In other words, the time constant  $R_A C$  controls the output pulse width.

When the applied voltage to the capacitor C1 reaches  $2 V_{CC}/3$ , the comparator on the trigger terminal resets the flip-flop, turning the discharging transistor on. At this time, C1 begins to discharge and the timer output converts to low. In this way, the timer operating in the monostable repeats the above process. Figure 3 shows the time constant relationship based on  $R_A$  and C. Figure 4 shows the general waveforms during the monostable operation.

It must be noted that, for a normal operation, the trigger pulse voltage needs to maintain a minimum of  $V_{CC}/3$  before the timer output turns low. That is, although the output remains unaffected even if a different trigger pulse is applied

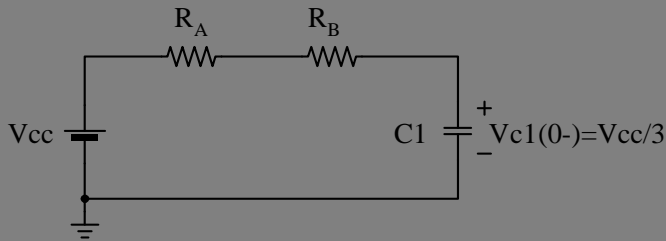


**Figure 8. Waveforms of Astable Operation**

An astable timer operation is achieved by adding resistor  $R_B$  to Figure 2 and configuring as shown on Figure 6. In the astable operation, the trigger terminal and the threshold terminal are connected so that a self-trigger is formed, operating as a multi-vibrator. When the timer output is high, its internal discharging transistor turns off and the  $V_{C1}$  increases by exponential function with the time constant  $(R_A + R_B) \cdot C$ .

When the  $V_{C1}$ , or the threshold voltage, reaches  $2 V_{CC}/3$ ; the comparator output on the trigger terminal becomes high, resetting the F/F and causing the timer output to become low. This turns on the discharging transistor and the  $C1$  discharges through the discharging channel formed by  $R_B$  and the discharging transistor. When the  $V_{C1}$  falls below  $V_{CC}/3$ , the comparator output on the trigger terminal becomes high and the timer output becomes high again. The discharging transistor turns off and the  $V_{C1}$  rises again.

In the above process, the section where the timer output is high is the time it takes for the  $V_{C1}$  to rise from  $V_{CC}/3$  to  $2 V_{CC}/3$ , and the section where the timer output is low is the time it takes for the  $V_{C1}$  to drop from  $2 V_{CC}/3$  to  $V_{CC}/3$ . When timer output is high, the equivalent circuit for charging capacitor  $C1$  is as follows:



$$C_1 \frac{dv_{c1}}{dt} = \frac{V_{CC} - V(0-)}{R_A + R_B} \quad (1)$$

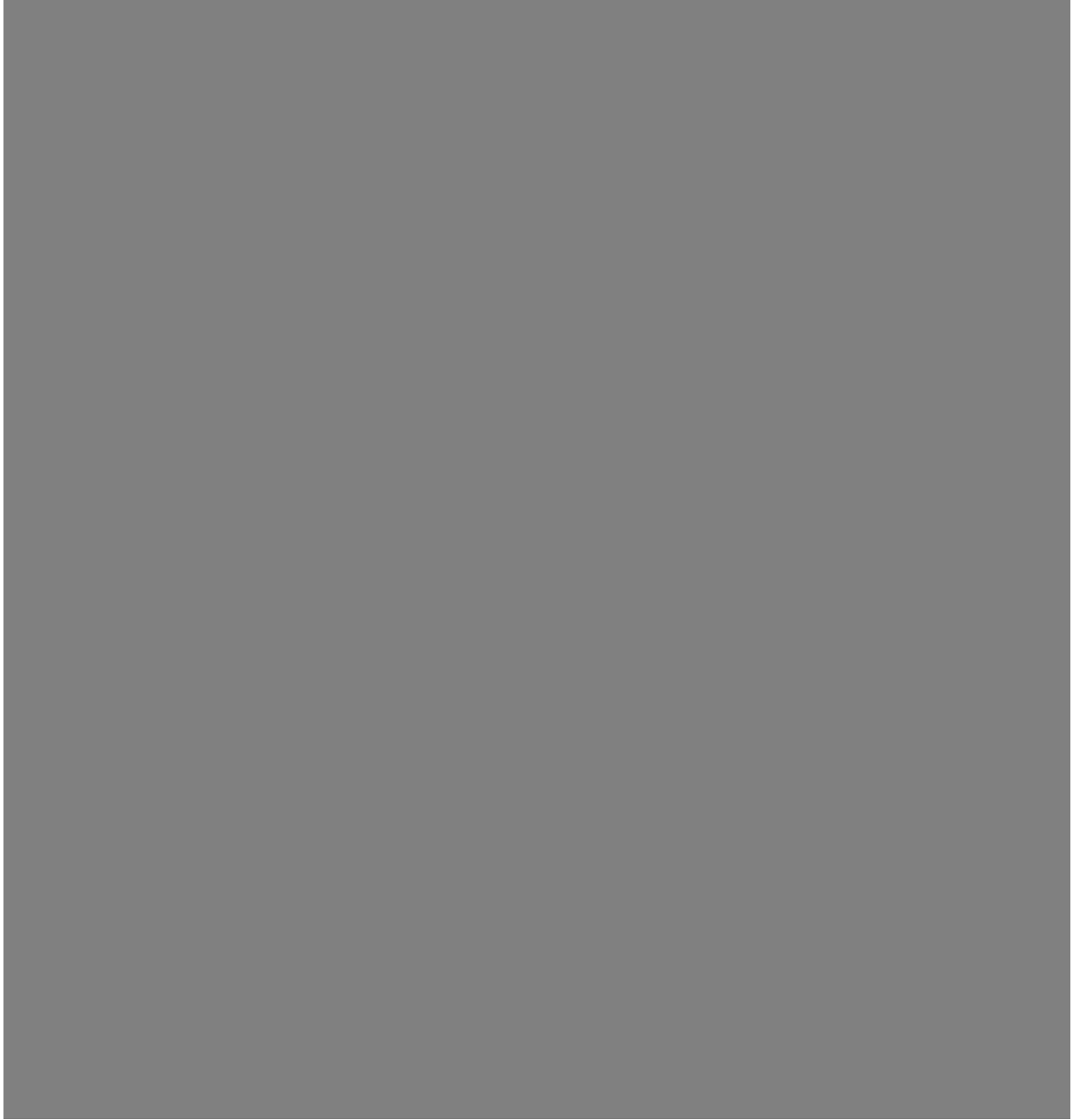
$$V_{C1}(0+) = V_{CC}/3 \quad (2)$$

$$V_{C1}(t) = V_{CC} \left( 1 - \frac{2}{3} e^{-\frac{t}{(R_A + R_B)C_1}} \right) \quad (3)$$

Since the duration of the timer output high state ( $t_H$ ) is the amount of time it takes for the  $V_{C1}(t)$  to reach  $2 V_{CC}/3$ ,

$$V_{C1}(t) = \frac{2}{3} V_{CC} = V_{CC} \left( 1 - \frac{2}{3} e^{-\frac{t_H}{(R_A + R_B)C_1}} \right) \quad (4)$$

$$t_H = C_1(R_A + R_B) \ln 2 = 0.693(R_A + R_B)C_1 \quad (5)$$





### 3. Frequency Divider

By adjusting the length of the timing cycle, the basic circuit of Figure 1 can be made to operate as a frequency divider. Figure 9. illustrates a divide-by-three circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

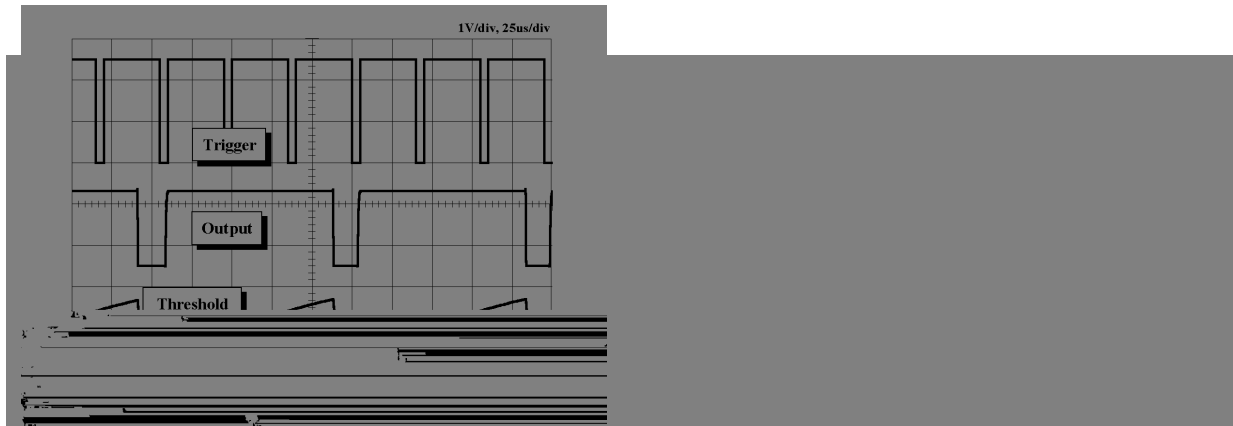


Figure 9. Waveforms of Frequency Divider Operation

### 4. Pulse Width Modulation

The timer output waveform may be changed by modulating the control voltage applied to the timer's pin 5 and changing the reference of the timer's internal comparators. Figure 10 illustrates the pulse width modulation circuit.

When the continuous trigger pulse train is applied in the monostable mode, the timer output width is modulated according to the signal applied to the control terminal. Sine wave, as well as other waveforms, may be applied as a signal to the control terminal. Figure 11 shows the example of pulse width modulation waveform.

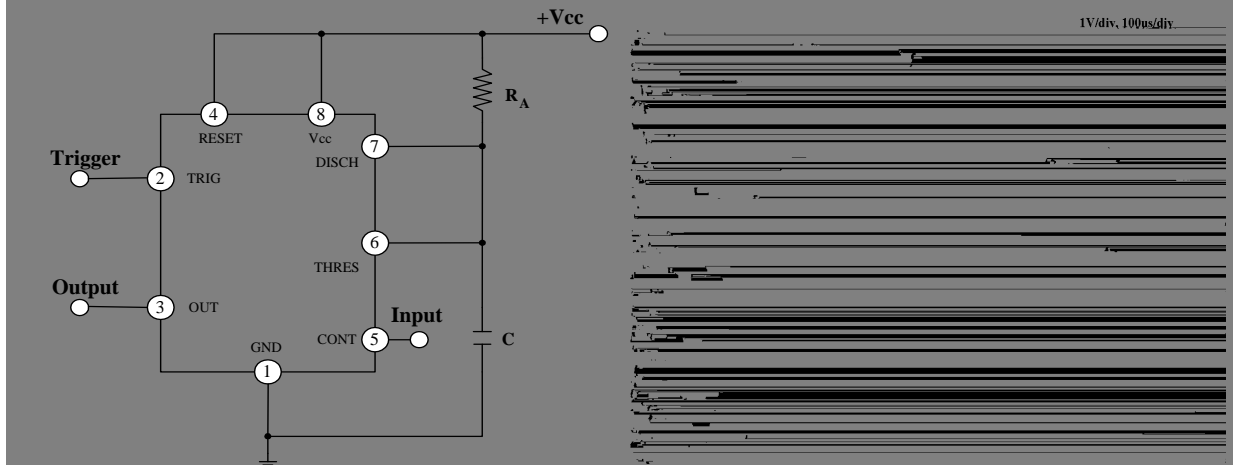


Figure 10. Circuit for Pulse Width Modulation

Figure 11. Waveforms of Pulse Width Modulation



In Figure 14, current source is created by PNP transistor Q1 and resistor R1, R2, and R<sub>E</sub>.

For example, if  $V_{CC} = 15\text{ V}$ ,  $R_E = 20\text{ k}\Omega$ ,  $R_1 = 5\text{ k}\Omega$ ,  $R_2 = 10\text{ k}\Omega$ , and  $V_{BE} = 0.7\text{ V}$ ,  
 $V_E = 0.7\text{ V} + 10\text{ V} = 10.7\text{ V}$ , and  
 $I_C = (15 - 10.7) / 20\text{ k} = 0.215\text{ mA}$ .

When the trigger starts in a timer configured as shown in Figure 14, the current flowing through capacitor C1 becomes a constant current generated by PNP transistor and resistors.



**Physical Dimensions** (continued)




**Figure 17. 8-Lead, SOIC, JEDEC MS-012, 150" NARROW BODY**

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