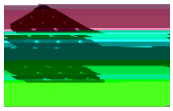
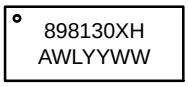
Advance Information



WLCSP36
CASE 567ZU

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
LC898130DP1XHTBG	WLCSP36 (Pb−Free)	4,000 / Tape & Reel
LC898130DPNXHTBG	WLCSP36 (Pb−Free)	4,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Overview

This is a system LSI integrating an on−chip 32bit DSP, a FLASH ROM and peripherals including analog circuits for OIS (Optical Image Stabilization) / Closed Loop−AF (Auto Focus) and Zoom control, constant current drivers and PIEZO drivers.

Features

- On−chip 32bit DSP
  - Built−in Software for Digital Servo Filter
  - Built−in Software for Gyro Filter
- Memory
  - Flash Memory
  - Program ROM
  - Program SRAM
  - Data SRAM
- Peripherals
  - AD Converter
  - DA Converter
  - 2−wire Serial I/F Circuit
    (The Communication Protocol is Compatible with I^2C)
  - Hall/MR Bias Circuit
  - VGA (Hall/MR Amp)
  - OSC (Oscillator)
  - LDO (Low Drop−Out Regulator)
  - Digital Gyro I/F (SPI)
  - Interrupt I/F
  - PLL
  - Temperature Sensor
- Driver
  - OIS/CL−AF and Zoom/PIEZO (Bi−direction)
    Constant Current Linear Driver (x2ch, I_{full} = 200 mA)
  - PIEZO (Di−direction)

AD/DA/VGA/LDO/OSC/Flash/PLL/Temp. Sensor:
AVDD = 2.7 V to 3.6 V
- Driver: V_M = 2.7 V to 3.6 V
- 1.8 V I/O: I_{OVDD} = 1.7 V to 3.6 V
- Core Logic: Generated by On−chip LDO
  Connect 1 μF Capacitor to LDPO Pin

BLOCK DIAGRAM

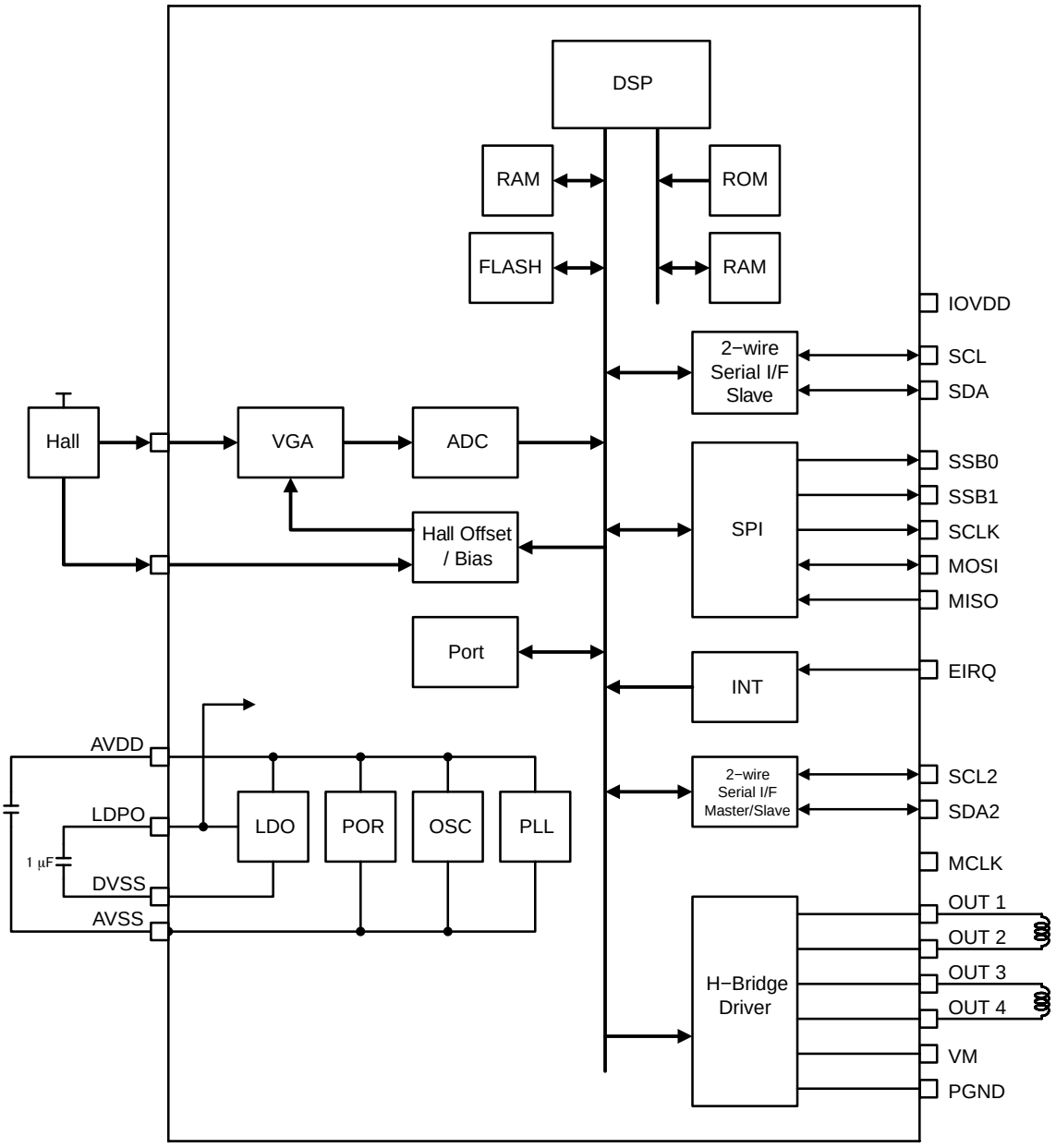


Figure 1. Block Diagram

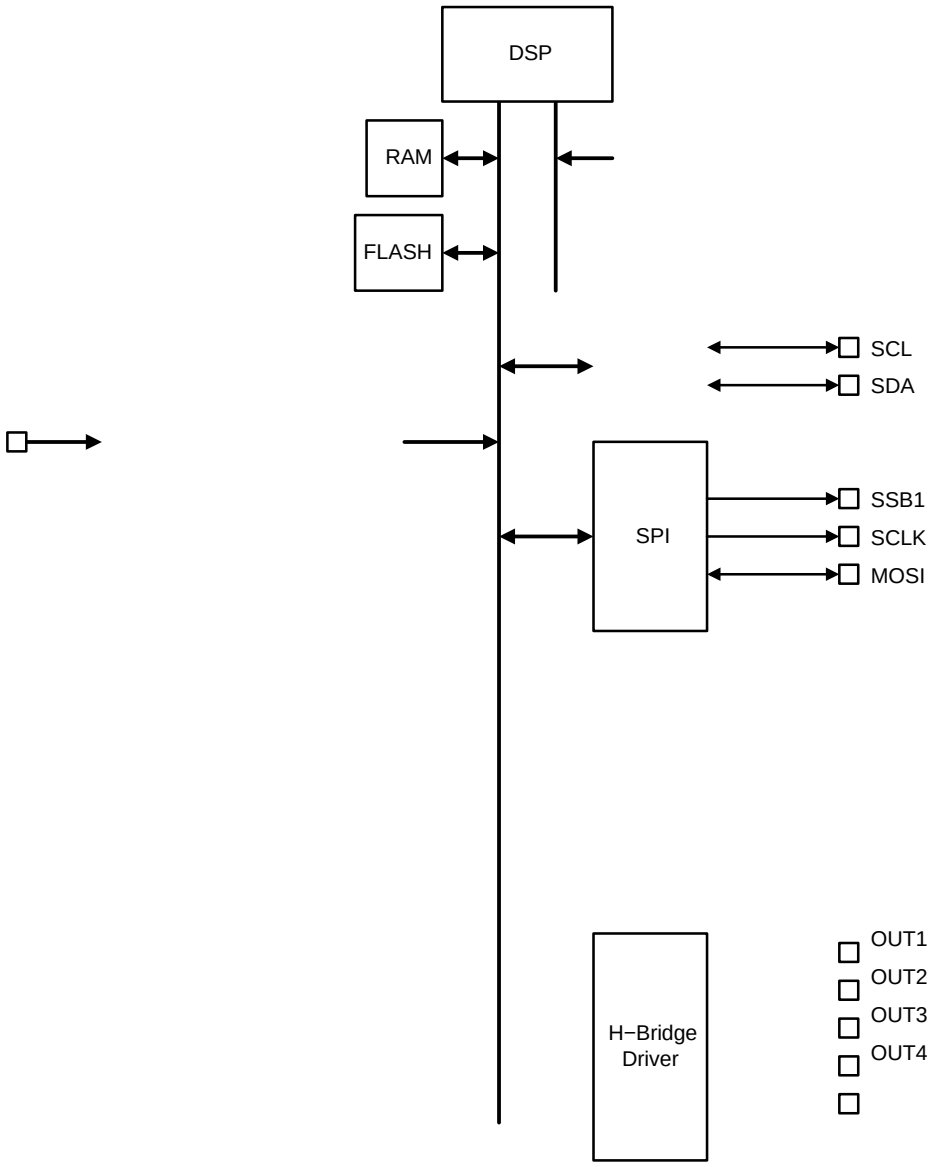


Figure 2. Block Diagram

PIN LAYOUT

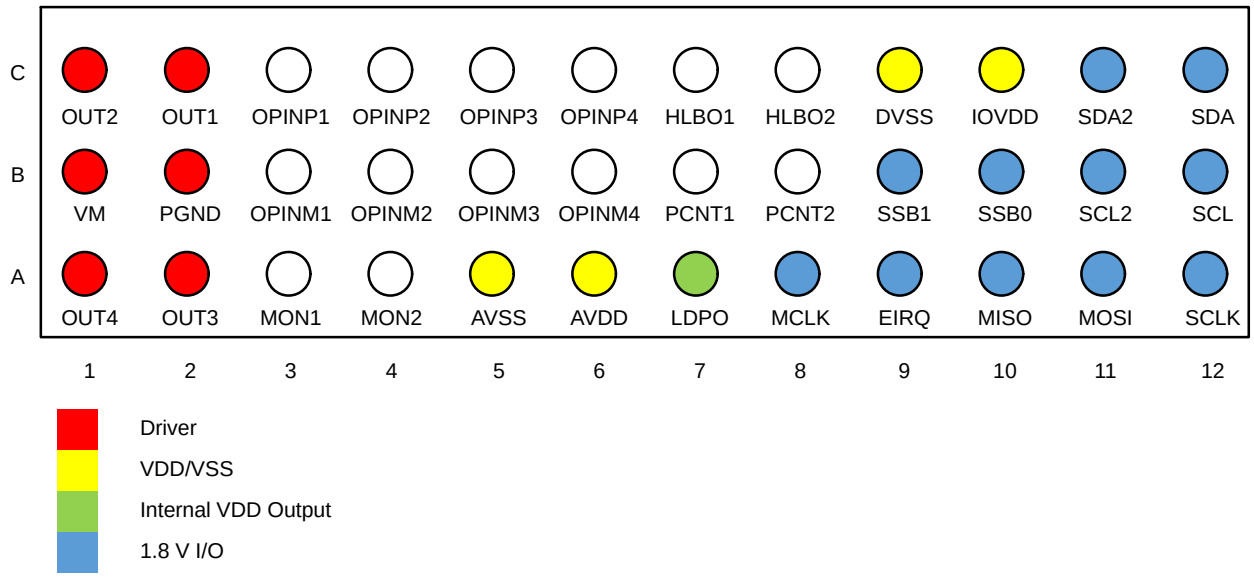


Figure 3. Pin Layout (Bottom View)

PIN DESCRIPTION

PIN DESCRIPTION

No.	Pin	I/O	I/O Pwr	Function	Init
1	MON1	B	AVDD	Servo Monitor Analog In/Out	Z
2	MON2	B	AVDD	Servo Monitor Analog In/Out	Z
3	SCL	B	IOVDD	2−wire serial HOST I/F Clock Slave	Z
4	SDA	B	IOVDD	2−wire serial HOST I/F Data Slave	Z
5	SSB0	B	IOVDD	Digital Gyro Data I/F Chip Select 0 Out (3/4−wire Master)	Z
6	SCLK	B	IOVDD	Digital Gyro Data I/F Clock Out (3/4−wire Master)	Z
7	MOSI	B	IOVDD	Digital Gyro Data I/F Data InOut (3−wire Master) Digital Gyro Data I/F Data Out (4−wire Master)	Z
8	MISO	B	IOVDD	Digital Gyro Data I/F Data In (4−wire Master) SSB2 SELADR	U
9	EIRQ	B	IOVDD	Interrupt Input	Z
10	MCLK	B	IOVDD	Master Clock	Z
11	SSB1	B	IOVDD	Digital Gyro Data I/F Chip Select 1 Out (3/4−wire Master)	Z
12	SCL2	B	IOVDD	2−wire serial I/F Clock Master/Slave	Z
13	SDA2	B	IOVDD	2−wire serial I/F Data Master/Slave	Z
14	HLBO1	O	AVDD	Hall/MR Bias Output 1	Z
15	HLBO2	O	AVDD	Hall/MR Bias Output 2	Z
16	PCNT1	O	AVDD	External Driver Power Control 1	Z
17	PCNT2	O	AVDD	External Driver Power Control 2	Z
18	OPINM1	I	AVDD	VGA (Hall/MR Amp) Input Minus 1	−
19			AVDD	VGA (Hall/MR Amp) Input Plus 1	−
20	OPINM2	I	AVDD	VGA (Hall/MR Amp) Input Minus 2	−
21			AVDD	VGA (Hall/MR Amp) Input Plus 2	−
22	OPINM3	I	AVDD	VGA Input Minus 3	−
24	OPINM4	I	AVDD	VGA Input Minus 4	−
25			AVDD	VGA (MR Amp) Input Plus 4	−
26	OUT1	O	VM	OIS Driver Output 1	Z
27	OUT2	O	VM	OIS Driver Output 2	Z
28	OUT3	O	VM	OIS Driver Output 3	Z
29	OUT4	O	VM	OIS Driver Output 4	Z
30	AVDD	P		Analog Power (2.7 V to 3.6 V)	−
31	AVSS	P		Analog GND	−
32	VM	P		Driver Power (2.7 V to 3.6 V)	−
33	PGND	P		Driver GND	−
34	IOVDD	P		I/O Power (1.7 V to 3.6 V)	−
35	DVSS	P		Digital GND	−
36	LDPO	P		Internal 1.38 V LDO Power Output	−

NOTE: Z: Hi−Z
U: Internal Pull

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (AVSS = 0 V, PGND = 0 V, DVSS = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Power Supply Voltage	V_{AD} max	$T_A \le 25°C$	−0.3 to 4.6	V
	V_M max	$T_A \le 25°C$	−0.3 to 4.6	V
	V_{IO} max	$T_A \le 25°C$	−0.3 to 4.6	V
Input/Output Voltage	V_{AI}, V_{AO}	$T_A \le 25°C$	−0.3 to V_{AD} + 0.3	V
	V_{MI}, V_{MO}	$T_A \le 25°C$	−0.3 to V_M + 0.3	V
	V_{II}, V_{IOO}	$T_A \le 25°C$	−0.3 to V_{IO} + 0.3	V
Storage Temperature	T_{stg}		−55 to 125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ALLOWABLE OPERATING RATINGS (T_A = −40 to 85°C, AVSS = 0 V, PGND = 0 V, DVSS = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
3.0 V POWER SUPPLY (AVDD)					
Power Supply Voltage	V_{AD}	2.7	2.8	3.6	V
Input Voltage Range	V_{INA}	0	−	V_{AD}	V
3.0 V POWER SUPPLY (VM)					
Power Supply Voltage	V_M	2.7	2.8	3.6	V
Input Voltage Range	V_{INM}	0	−	V_M	V
1.8 V POWER SUPPLY (IOVDD)					
Power Supply Voltage	V_{IO}	1.7	1.8	3.6	V
Input Voltage Range	V_{INI}	0	−	V_{IO}	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC CHARACTERISTICS: INPUT/OUTPUT

(T_A = −40 to 85°C, AVSS = 0 V, PGND = 0 V, DVSS = 0 V, AVDD = 2.7 to 3.6 V, IOVDD = 1.7 to 3.6 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit

A1[DC 071 13.209 rethe)Tj3PP9Par

DC CHARACTERISTICS: INPUT/OUTPUT

AC CHARACTERISTICS

Power Supply Timing

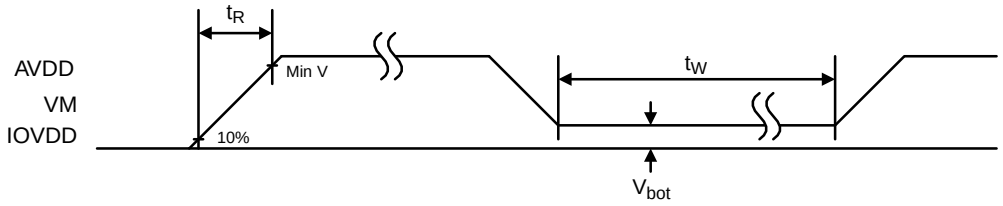


Figure 4. V_{DD} Supply Timing

Table 1.

Item	Symbol	Min	Typ	Max	Unit
Rise Time	t_R	–	–	3	ms
Wait Time	t_W	100	–	–	ms
Bottom Voltage	V_{bot}	–	–	0.2	V

Injection order between AVDD, VM and IOVDD is below.

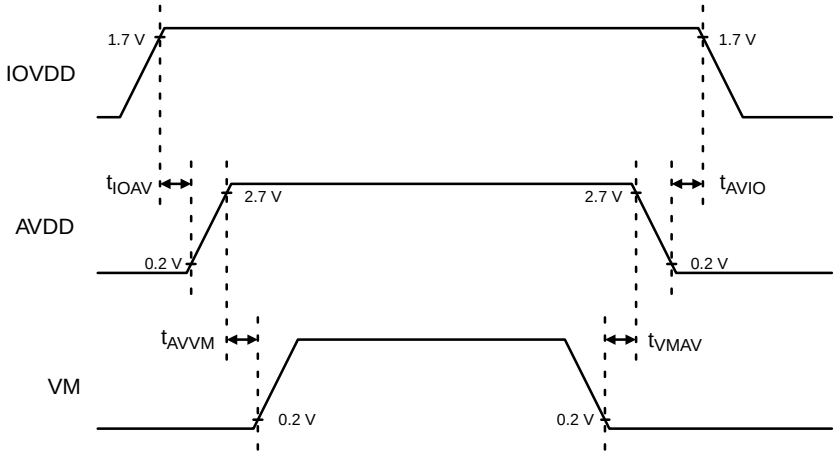


Figure 5. Injection Order between AVDD, VM and IOVDD

Table 2.

Item	Symbol

PACKAGE DIMENSIONS

WLCSP36 1.295x4.74x0.33
CASE 567ZU
ISSUE O