



# LC898121XA

## BLOCK DIAGRAM

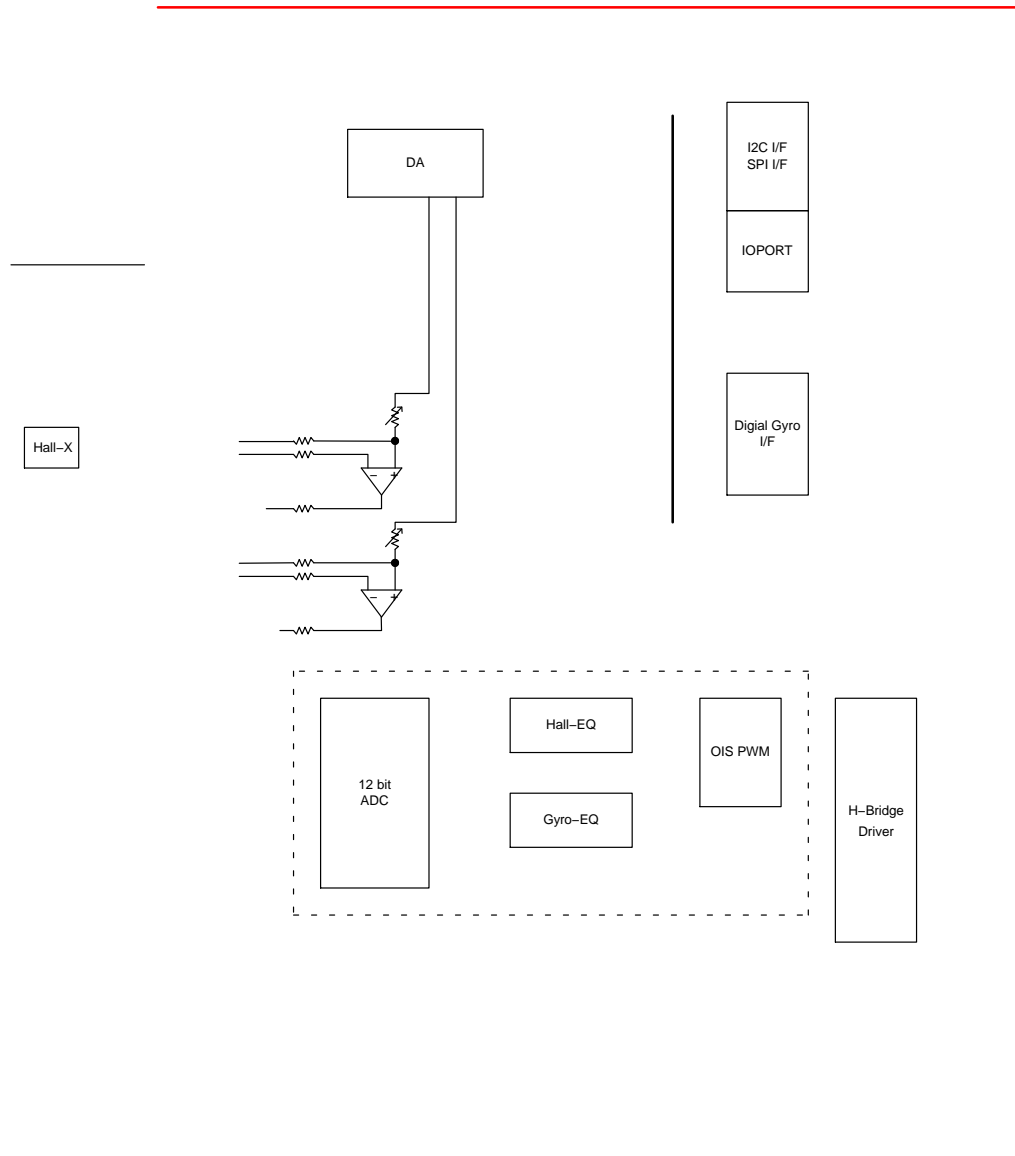


Figure 1. Example of Wiring Diagram [Hall] in LC898121XA (WLP40)

# LC898121XA

## PIN ASSIGNMENT

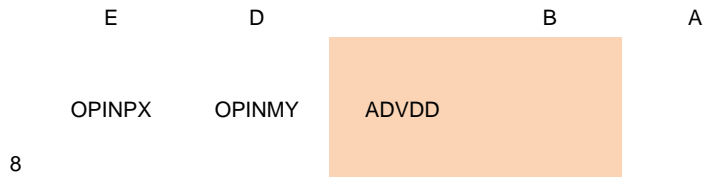


Figure 2. WLP40 Bottom View

# LC898121XA

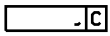
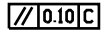
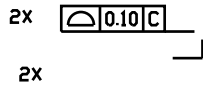
## PIN DESCRIPTION (Type – I: INPUT, O: OUTPUT, B: BIDIRECTION, P: Power)

Ball No	Pin Name	Type	Description
A1	OUT1	O	Driver Output
A2	VM	P	Driver VDD (2.6 V to 5.5 V)
A3	DVDD30	P	Logic 3 V VDD (2.6 V to 3.6 V)
A4	DVDD18	P	LDO Power supply out (Logic Core VDD (typ 1.8 V))
A5	I2CDT	B	I2C_IF data (B) / SPI IF data (I)
A6	I2CCK	I	I2C_IF clock / SPI IF clock
A7	HYI	I	Hall–Y AD input
A8	HXI	I	Hall–X AD input
B1	OUT2	O	Driver output
B2	ZRESET	I	HardWafer Reset
B3	TEST	I	SPI & External clock case sets [1]. other cases set [0]
B4	SSB	B	SPI I/F Chip Select (I) / General–purpose IOPORT(B) / inner signal monitor (O)
B5	MISO	B	SPI I/F data (O) / inner signal monitor / General–purpose IOPORT
B6	DAOPVSS	P	DA&OpAmp VSS

B7

WLCSP40, 2.44x3.94  
CASE 567JB  
ISSUE A

DATE 20 DEC 2022



3.94 BSC  
2.44 BSC

A1

E  
D  
C  
B  
A

PACKAGE  
OUTLINE

RECOMMEN

2 3 4

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