

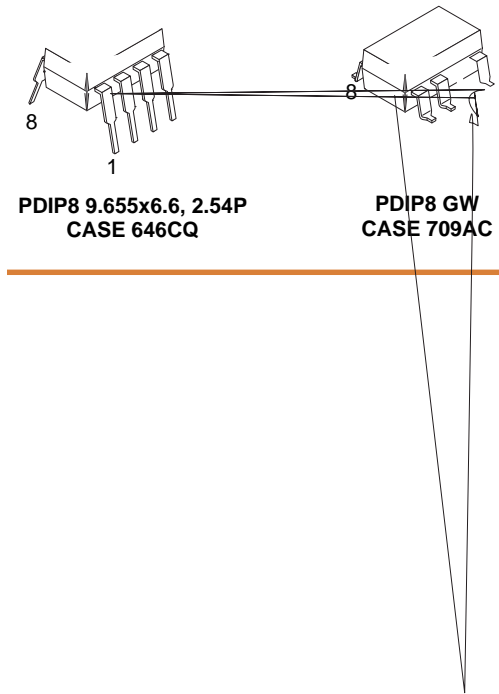
# AC/DC to Logic Interface Optocoupler

## HCPL3700M

### Description

### Features

### Applications



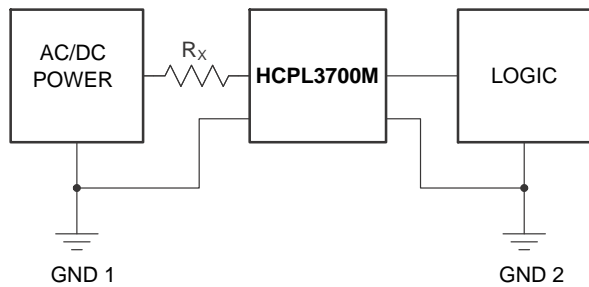



Figure 1. Schematic

### MARKING DIAGRAM



- 3700 = Device Number
- V = DIN EN/IEC60747-5-5 Option (only appears on component ordered with this option)
- XX = Two-Digit Year Code
- YY = Two-Digit Work Week
- B = Assembly Package Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

# HCPL3700M

**SAFETY AND INSULATION RATINGS** (As per DIN EN/IEC 60747-5-5, this optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.)

Parameter	Characteristics
Installation Classifications per DIN VDE 0110/1.89 Table 1, For Rated Mains Voltage	< 150 V

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## ELECTRICAL CHARACTERISTICS ( $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.
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## SWITCHING CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5\text{ V}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$t_{PHL}$	Propagation Delay Time (to Output Low Level)	$R_L = 4.7\text{ k}\Omega$ , $C_L = 30\text{ pF}$ (Note 7)		6.0	15	$\mu\text{s}$
$t_{PLH}$	Propagation Delay Time (to Output High Level)	$R_L = 4.7\text{ k}\Omega$ , $C_L = 30\text{ pF}$ (Note 7)		25.0	40	$\mu\text{s}$
$t_R$	Output Rise Time (10%–90%)	$R_L = 4.7\text{ k}\Omega$ , $C_L = 30\text{ pF}$		45		$\mu\text{s}$
$t_F$	Output Fall Time (90%–10%)	$R_L = 4.7\text{ k}\Omega$ , $C_L = 30\text{ pF}$		0.5		$\mu\text{s}$
$ICM_{HI}$	Common Mode Transient Immunity (at Output High Level)	$I_{IN} = 0\text{ mA}$ , $R_L = 4.7\text{ k}\Omega$ , $V_{Omin} = 2.0\text{ V}$ , $V_{CM} = 1400\text{ V}$ (Notes 8, 9)		4000		$\text{V}/\mu\text{s}$
$ICM_{LI}$	Common Mode Transient Immunity (at Output Low Level)	$I_{IN} = 3.11\text{ mA}$ , $R_L = 4.7\text{ k}\Omega$ , $V_{Omax} = 0.8\text{ V}$ , $V_{CM} = 1400\text{ V}$ (Notes 8, 9)		600		$\text{V}/\mu\text{s}$

## ISOLATION CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{ISO}$	Withstand Isolation Voltage	$RH \leq 50\%$ , $I_{I-O} \leq 10\text{ }\mu\text{A}$ , $t = 1\text{ min}$ , $f = 50\text{ Hz}$ (Note 10, 11)	5,000	–	–	$\text{VAC}_{RMS}$
$R_{I-O}$	Resistance (Input to Output)	$V_{IO} = 500\text{ V}_{DC}$ (Note 10)	–	$10^{12}$	–	$\Omega$
$C_{I-O}$	Capacitance (Input to Output)	$f = 1\text{ MHz}$ , $V_{IO} = 0\text{ V}_{DC}$	–	0.6	–	$\text{pF}$

- $T_{PHL}$  propagation delay is measured from the 2.5 V level of the leading edge of a 5.0 V input pulse (1  $\mu\text{s}$  rise time) to the 1.5 V level on the leading edge of the output pulse.  $T_{PLH}$  propagation delay is measured on the trailing edges of the input and output pulse. (Refer to Fig. 10)
- Common mode transient immunity in logic high level is the maximum tolerable (positive)  $dV_{cm}/dt$  on the leading edge of the common mode pulse signal  $V_{CM}$ , to assure that the output will remain in a logic high state (i.e.,  $V_O > 2.0\text{ V}$ ). Common mode transient immunity in logic low level is the maximum tolerable (negative)  $dV_{cm}/dt$  on the trailing edge of the common mode pulse signal,  $V_{CM}$ , to assure that the output will remain in a logic low state (i.e.,  $V_O < 0.8\text{ V}$ ). Refer to Fig. 11.
- In applications where  $dV_{cm}/dt$  may exceed 50,000  $\text{V}/\mu\text{s}$  (Such as static discharge), a series resistor,  $R_{CC}$ , should be included to protect the detector chip from destructive surge currents. The recommended value for  $R_{CC}$  is 240  $\Omega$  per volt of allowable drop in  $V_{CC}$ .

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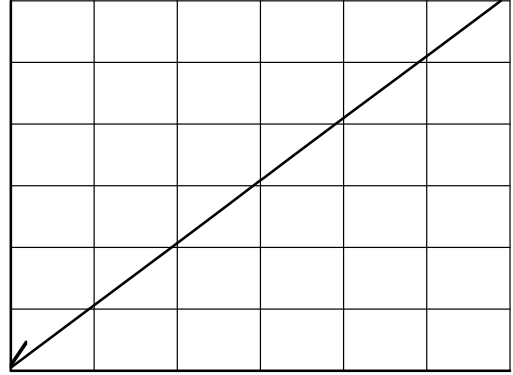
## TYPICAL PERFORMANCE CURVES

$I_{IN}$ , INPUT CURRENT (mA)

$T_A$ , TEMPERATURE (°C)

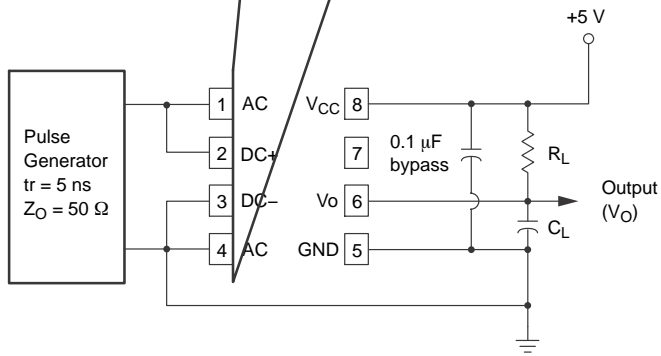
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## TYPICAL PERFORMANCE CURVES (continued)



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## TEST CIRCUITS



$V_{IN}$   
 Pulse Amplitude = 50 V  
 Pulse Width = 1 ms  
 $f = 100 \text{ Hz}$   
 $T_r = T_f = 1.0 \mu\text{s} (10\% - 90\%)$

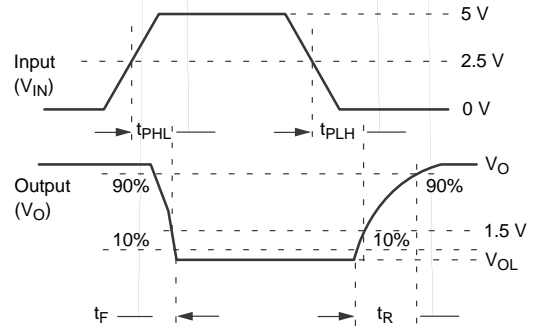


Figure 10. Switching Test Circuit

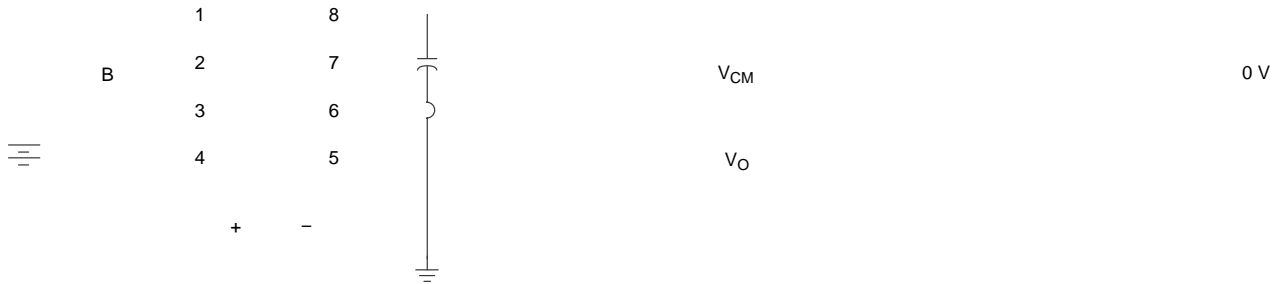
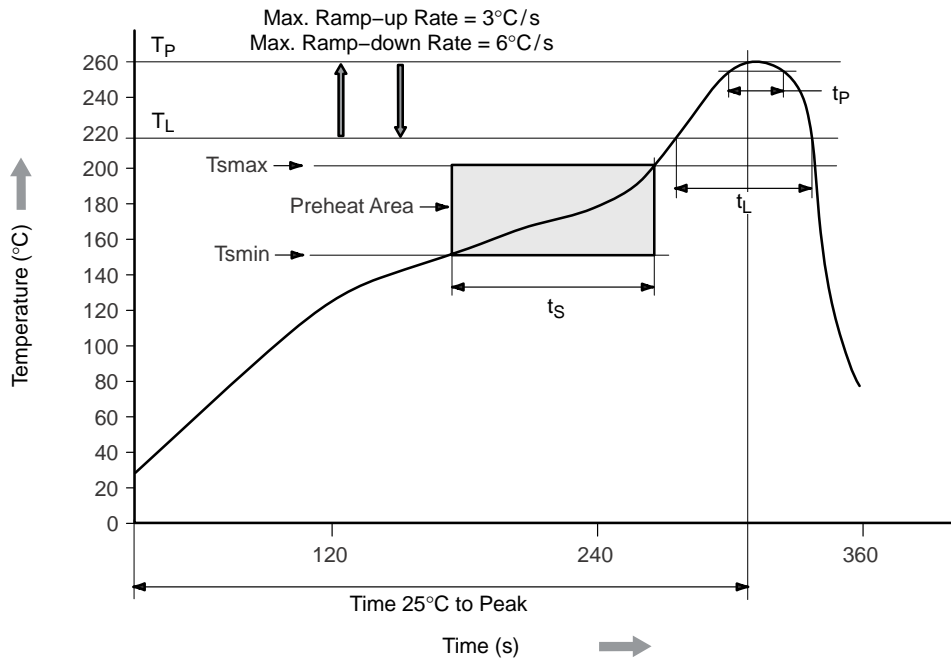


Figure 11. Test Circuit for Common Mode Transient Immunity and Typical Waveforms



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## REFLOW PROFILE



Profile Feature	Pb-Free Assembly Profile
Temperature Minimum (T <sub>smin</sub> )	150°C
Temperature Maximum (T <sub>smax</sub> )	200°C
Time (t <sub>s</sub> ) from (T <sub>smin</sub> to T <sub>smax</sub> )	60 to 120 s
Ramp-up Rate (t <sub>L</sub> to t <sub>p</sub> )	3°C/s maximum
Liquidous Temperature (T <sub>L</sub> )	217°C
Time (t <sub>L</sub> ) Maintained Above (T <sub>L</sub> )	60 to 150 s
Peak Body Package Temperature	260°C +0°C/-5°C
Time (t <sub>p</sub> ) within 5°C of 260°C	30 s
Ramp-down Rate (T <sub>P</sub> to T <sub>L</sub> )	6°C/s maximum
Time 25°C to Peak Temperature	8 minutes maximum

Figure 12. Reflow Profile

# HCPL3700M

## ORDERING INFORMATION

Part Number	Package	Packing Method†
HCPL3700M	DIP 8-Pin	50 Units / Tube
HCPL3700SM		

PDIP8 9.655x6.6, 2.54P  
CASE 646CQ  
ISSUE O

DATE 18 SEP 2017

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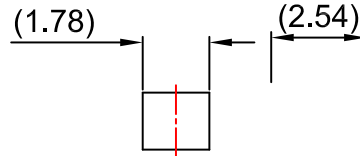
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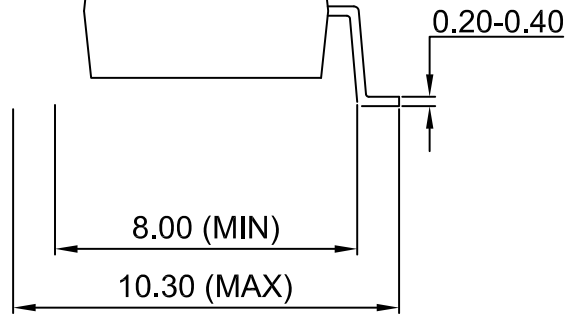
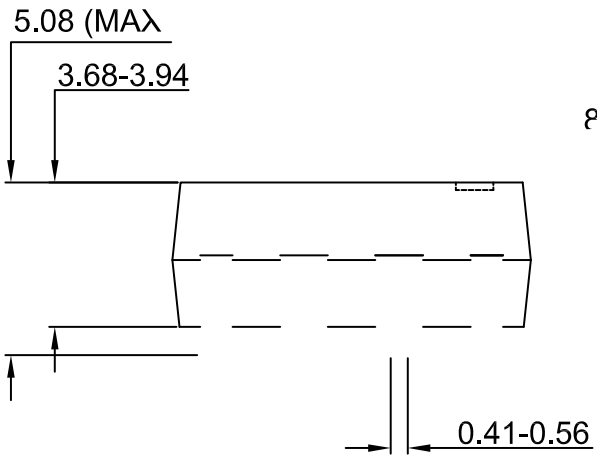
**PDIP8 GW**  
**CASE 709AC**  
**ISSUE O**

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