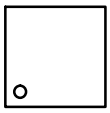
Dual Supply, 2-Bit Voltage Translator/Buffer/Repeater/Isolator for I²C Applications

FXMA2102

UQFN8, 1.4x1.2, 0.4P
CASE 523AS

UQFN8 1.6X1.6, 0.5P
CASE 523AY

MARKING DIAGRAM



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ORDERING INFORMATION

Description

The FXMA2102 is a high performance configurable dual voltage supply translator for bi directional voltage translation over a wide range of input and output voltages levels.

Intended for use as a voltage translator between I^2C Bus complaint masters and slaves.

The device is designed so that the A port tracks the V_{CCA} level and the B port tracks the V_{CCB} level. This allows for bi directional A/B port voltage translation between any two levels from 1.65 V to 5.5 V. V_{CCA} can equal V_{CCB} from 1.65 V to 5.5 V. The OE pin is referenced to V_{CCA}.

Either V_{CC} can be powered up first. Internal power down control circuits place the device in 3 state if either VCC is removed.

The two ports of the device have automatic direction sense capability. Either port may sense an input signal and transfer it as an output signal to the other port.

Features

Bi Directional Interface between AnVt /TT7 1 Tf10 0 0 10 70.2992 261.4678 Tm-0006 Tc(Supports I)Tβ 0 0 8 111.3449 264.5292 Tm(

2 kV CDM (per JESD22 C101)

BLOCK DIAGRAM

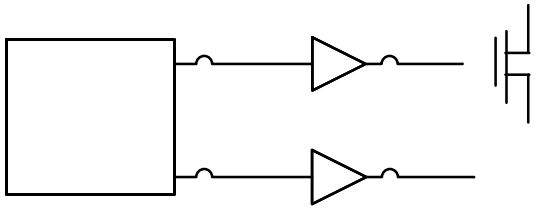

Figure 1. Block Diagram, 1 of 2 Channels

PIN CONFIGURATION

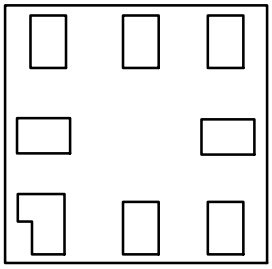

Figure 2. MicroPak (Top−Through View)

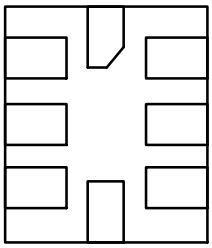

Figure 3. UMLP (Top−Through View)

PIN DEFINITIONS

Pin No.	Name	Description
		−
	0	− −
	0	− −
		−

TRUTH TABLE

Control	
OE	Outputs
	−

0 0 −

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
		–			
		–			
			–		
			–		
			–		
			–		
			–		
		–	–		
		–	–		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
		–	–		
		–	–		

FUNCTIONAL DESCRIPTION

Power−Up/Power−Down Sequencing

FXM translators offer an advantage in that either V_{CC} may be powered up first. This benefit derives from the chip design. When either V_{CC} is at 0 V, outputs are in a high impedance state. The control input (OE) is designed to track the V_{CCA} supply. A pull down resistor tying OE to GND should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power up/ power down. The size of the pull down resistor is based upon the current sinking capability of the device driving the OE pin.

The recommended power up sequence is:

1. Apply power to the first V_{CC}.
2. Apply power to the second V_{CC}.
3. Drive the OE input HIGH to enable the device.

The recommended power down sequence is:

1. Drive OE input LOW to disable the device.
2. Remove power from either V_{CC}.
3. Remove power from other V_{CC}.

NOTE:

4. Alternatively, the OE pin can be hardwired to V_{CCA} to save GPIO pins. If OE is hardwired to V_{CCA}, either V_{CC} can be powered up or down first.

APPLICATION CIRCUIT

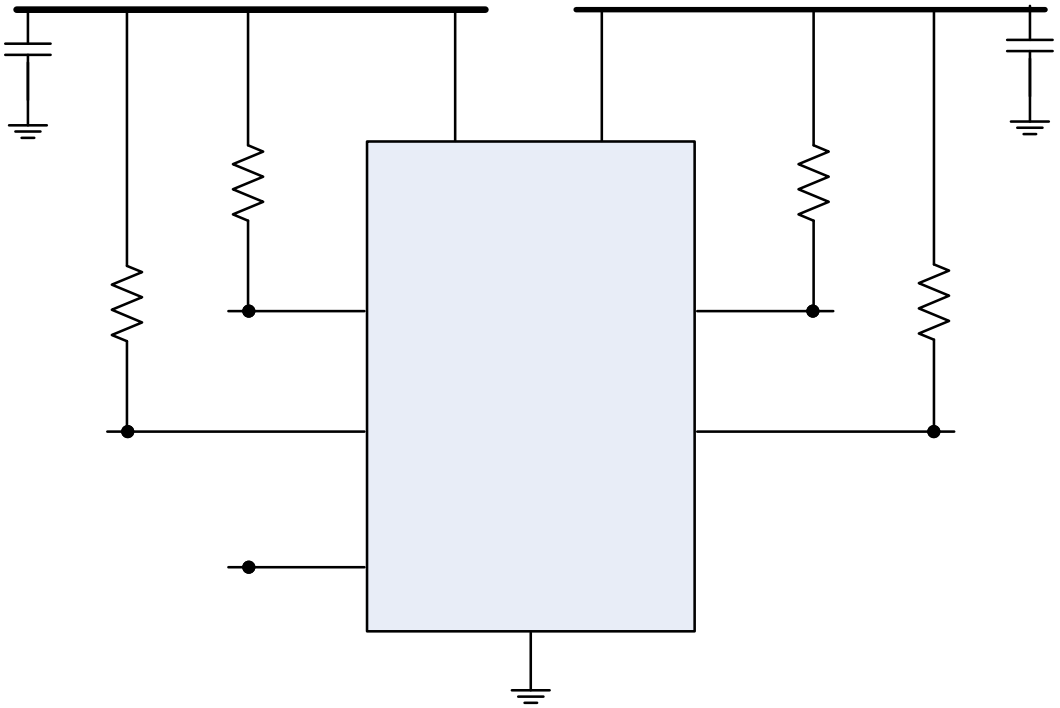

Figure 4. Application Circuit

APPLICATION NOTES

The FXMA2102 has open drain I/Os and requires external pull up resistors on the four data I/O pins, as shown in Figure 4. If a pair of data I/O pins (A_n/B_n) is not used, both pins should be tied to GND (or both to V_{CC}). In this case, pull down or pull up resistors are not required. The recommended values for the pull up resistors (RPU) are 1 kΩ to 10 kΩ; however, depending on the total bus capacitance, the user is free to vary the pull up resistor value to meet the maximum I^2C edge rate per the I^2C specification (UM10204 rev. 03, June 19, 2007). For example, the maximum edge rate (30% 70%) during fast mode (400 kbit/s) is 300 ns. If bus capacitance is approaching the maximum 400 pF, low er the RPU value to keep the rise time below 300 ns (Fast Mode). Section 7.1 of the I^2C specification provides an excellent guideline for pull up resistor sizing.

Theory of Operation

The FXMA2102 is designed for high performance level shifting and buffer / repeating in an I^2C application. Figure 1 shows that each bi directional channel contains two series Npassgates and two dynamic drivers. This hybrid architecture is highly beneficial in an I^2C application where auto direction is a necessity.

For example, during the following three I

1.65 V and a slave on the I^2C translator B port w ith a V_{CC} of 3.3 V, the maximum V_{IL} of the master is (1.65 V x 0.3) 495 mV. The slave could legally transmit a valid logic LOW of 0.4 V to the master.

If the I^2C translator's channel resistance is too high, the voltage drop across the translator could present a V_{IL} to the master greater than 495 mV. To complicate matters, the I^2C specification states that 6 mA of I_{OL} is recommended for bus capacitances approaching 400 pF. More I_{OL} increases the voltage drop across the I^2C translator. The I^2C application benefits w hen I^2C translators exhibit low V_{OL} performance. Figure 6 depicts typical FXMA2102 V_{OL} performance vs. the competition, given a 0.4 V V_{IL}.

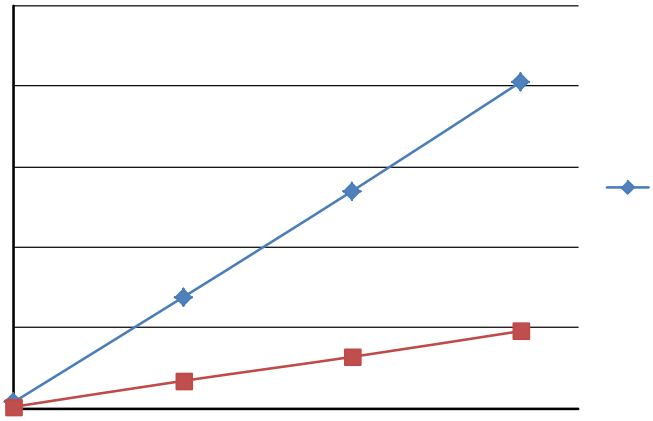

Figure 6. V_{OL} vs. I_{OL}

I^2C−Bus Isolation

The FXMA2102 supports I^2C

DYNAMIC OUTPUT ELECTRICAL CHARACTERISTICS

OUTPUT RISE / FALL TIME Ω –

Symbol	Parameter	V_{CCO} 4.5 to 5.5 V Typ	V_{CCO} 3.0 to 3.6 V Typ	V_{CCO} 2.3 to 2.7 V Typ	V_{CCO} 1.65 to 1.95 V Typ	Unit

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DYNAMIC OUTPUT ELECTRICAL CHARACTERISTICS

MAXIMUM DATA RATE Ω –

V_{CCA}	Direction	V_{CCB} 4.5 to 5.5 V Min	V_{CCB} 3.0 to 3.6 V Min	V_{CCB} 2.3 to 2.7 V Min	V_{CCB} 1.65 to 1.95 V Min	Unit

AC CHARACTERISTICS Ω –

Symbol	Parameter	V_{CCB} 4.5 to 5.5 V Typ	Max	3.0 to 3.6 V Typ	Max	2.3 to 2.7 V Typ	Max	1.65 to 1.95 V Typ	Max	Unit
V_{CCA} = 4.5 to 5.5 V										
			–		–		–		–	
V_{CCA} = 3.0 to 3.6 V										
			–		–		–		–	
V_{CCA} = 2.3 to 2.7 V										
			–		–		–		–	
V_{CCA} = 1.65 to 1.95 V										
			–		–		–		–	

– – – – *(see Figure 15)*

CAPACITANCE

Symbol	Parameter

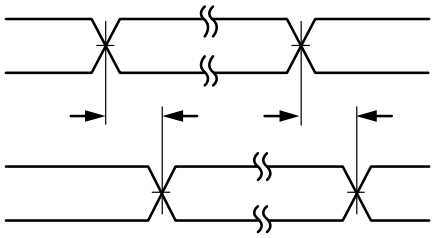
Table 1. PROPAGATION DELAY TABLE

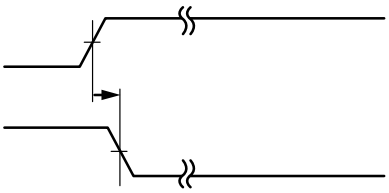
Test

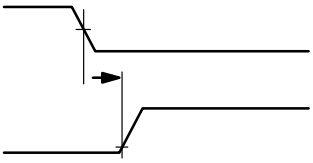
Table 2. AC LOAD TABLE

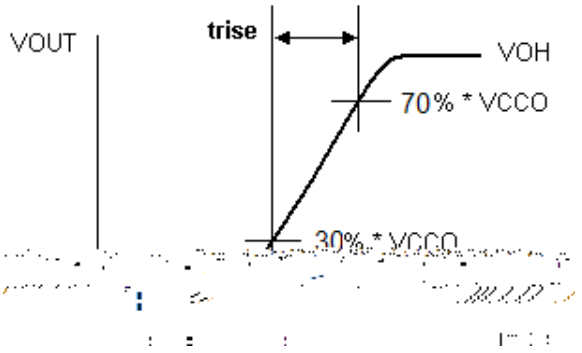
V_{CCO}	C_L	R_L

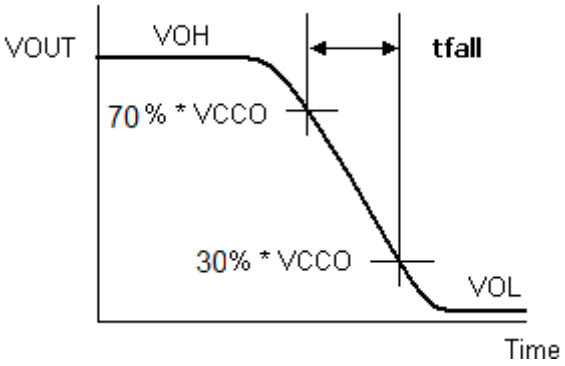
TIMING DIAGRAMS

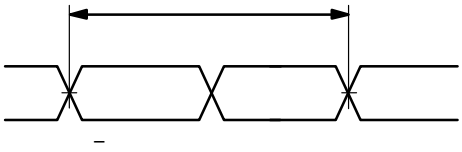












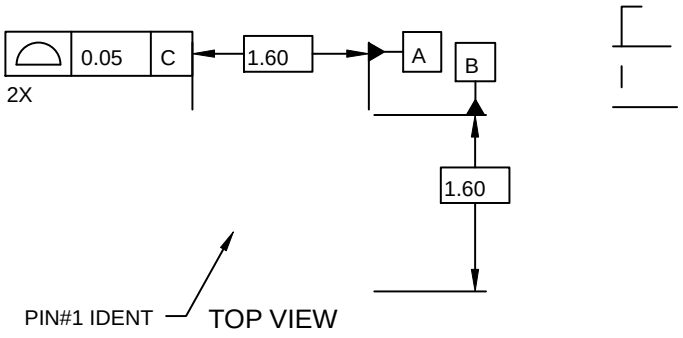
ORDERING INFORMATION

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
	–		– –	
			– –	

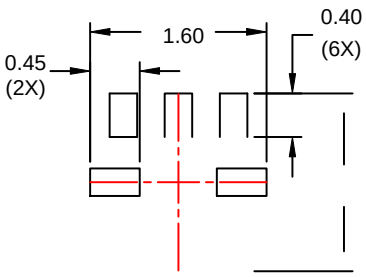
UQFN8, 1.40x1.20, 0.40P
CASE 523AS
ISSUE B

UQFN8 1.6X1.6, 0.5P
CASE 523AY
ISSUE O

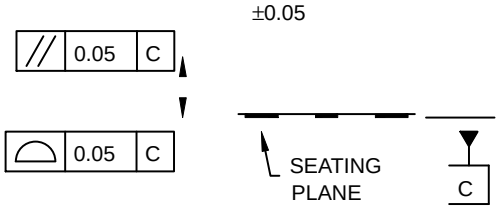
DATE 31 AUG 2016



TOP VIEW



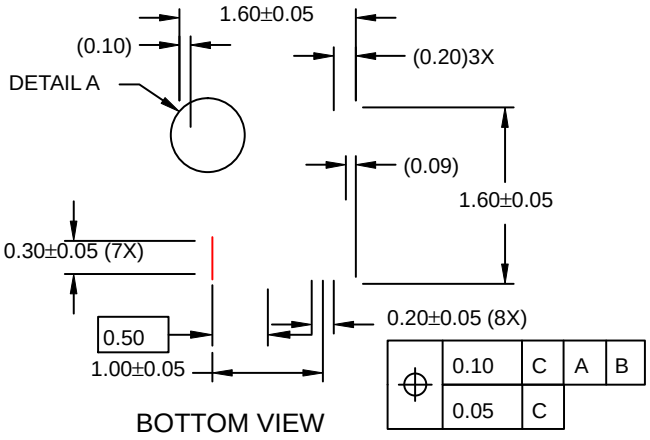
RECOMMENDED
LAND PATTERN



SIDE VIEW

NOTES:

A. PACKAGE CONFORMS TO JEDEC MO−



BOTTOM VIEW

DETAIL A
SCALE : 2X