Pin Configuration

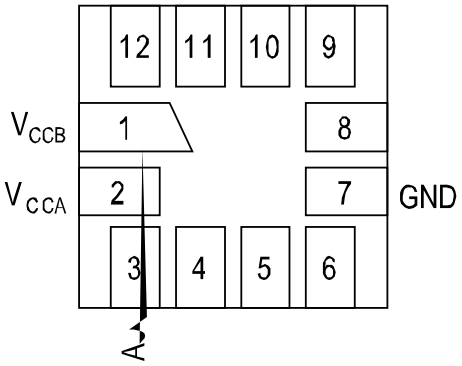


Figure 1. 16-Pin UMLP (Top Through View)

Figure 2. 12-Pin UMLP (Top Through View)

Pin Definitions

16 Pin #	12 Pin #	Name	Description
1	3	A0	A-Side Inputs or 3-State Outputs
2	4	A1	A-Side Inputs or 3-State Outputs
3	5	A2	A-Side Inputs or 3-State Outputs
4	6	A3	A-Side Inputs or 3-State Outputs
5		NC	No Connect
6,7	7	GND	Ground
8	8	/OE	Output Enable Input
9	9	B3	B-Side Inputs or 3-State Outputs
10	10	B2	B-Side Inputs or 3-State Outputs
11	11	B1	B-Side Inputs or 3-State Outputs
12	12	B0	B-Side Inputs or 3-State Outputs
13	1	V_{CCB}	B-Side Power Supply
14,15		NC	No Connect
16	2	V_{CCA}	A-Side Power Supply

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage	V_{CCA}	-0.5	4.6	V
		V_{CCB}	-0.5	4.6	
V_I	DC Input Voltage	I/O Ports A and B	-0.5	4.6	V
		Control Input (/OE)	-0.5	4.6	
V_O	Output Voltage[2]	Output 3-State	-0.5	4.6	V
		Output Active (A_n)	-0.5	V_{CCA} +0.5	
		Output Active (B_n)	-0.5	V_{CCB} +0.5	
I_{IK}					

Power-Up/Power-Down Sequence

FXL translators offer an advantage in that either V_{CC} may be powered up first. This benefit derives from the chip design. When either V_{CC} is at 0V, outputs are in a high-impedance state. The control input (/OE) is designed to track the V_{CCA} supply. A pull-up resistor tying /OE to V_{CCA} should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power-up or power-down. The size of the pull-up resistor is based upon the current-sinking capability of the device driving the /OE pin.

The recommended power-up sequence is:

1. Apply power to the first V_{CC}.
2. Apply power to the second V_{CC}.
3. Drive the /OE input LOW to enable the device.

The recommended power-down sequence is:

1. Drive /OE input HIGH to disable the device.
2. Remove power from either V_{CC}.
3. Remove power from other V_{CC}.

Pull-Up/Pull-Down Resistors

Do not use pull-up or pull-down resistors

DC Electrical Characteristics

T_A=-40 to 85°C

Symbol	Parameter	Conditions	V_{CCA} (V)	V_{CCB} (V)	Min.	Typ.	Max.	Units
V_{IHA}	High-Level Input Voltage	Data Inputs A_n Control Pin /OE	2.70 to 3.60	1.10 to 3.60	2.00			V
			2.30 to 2.70		1.60			

FXLA104 — Low-Voltage Dual-Supply 4-Bit Voltage Translator

Dynamic Output Electrical Characteristic

A Port (A_n)

Output Load: C_L=15pF, $R_L \geq M\Omega$ ($C_{I/O}$=4pF), T_A=-40 to 85°C

	V_{CCA}=3.0V to 3.6V	V_{CCA}=2.3V to 2.7V	V_{CCA}=1.65V to 1.95V	V_{CCA}=1.4V to 1.6V	V_{CCA}=1.1V to 1.2V	
05w2 4. Tc8 re Symbol 99.Pa2605w2 4. Tc8 re504 .275 0 w 9L)Tj 8[5 Tc4 1w 6t48 0(Tj Td663 1.1 87J 0 57m38c Units 23 4(B14 4(l)1.3						

AC Characteristics

V_{CCA} = 3.0V to 3.6V, T_A=-40 to 85°C

Symbol	Parameter	V_{CCB}=3.0V to 3.6V		V_{CCB}=2.3V to 2.7V		V_{CCB}=1.65V to 1.95V		V_{CCB}=1.4V to 1.6V		V_{CCB}=1.1V to 1.3V	Units
		Min.	Max.	Min.	Max.	Min.	Max	Min.	Max.	Typ.	
t_{PLH},t_{PHL}	A to B	0.2	4.0	0.3	4.2	0.5	5.4	0.6	6.8	6.9	ns
	B to A	0.2	4.0	0.2	4.1	0.3	5.0	0.5	6.0	4.5	ns
t_{PZL},t_{PZH}	/OE to A, /OE to B		1.7		1.7		1.7		1.7	1.7	µs
t_{SKEW}	A Port, B Port(11)		0.5		0.5		0.5		1.0	1.0	ns

V_{CCA} = 2.3V to 2.7V, T_A=-40 to 85°C

Symbol	Parameter	V_{CCB}=3.0V to 3.6V		V_{CCB}=2.3V to 2.7V		V_{CCB}=1.65V to 1.95V		V_{CCB}=1.4V to 1.6V		V_{CCB}=1.1V to 1.3V	Units
		Min.	Max.	Min.	Max.	Min.	Max	Min.	Max.	Typ.	
t_{PLH},t_{PHL}	A to B	0.2	4.1	0.4	4.5	0.5	5.6	0.8	6.9	7.0	ns
	B to A	0.3	4.2	0.4	4.5	0.5	5.5	0.5	6.5	4.8	ns

t_{PZL},t

Maximum Data Rate[13, 14]

T_A=-40 to 85°C

V_{CCA}	V_{CCB}=3.0V to 3.6V	V_{CCB}=2.3V to 2.7V	V_{CCB}=1.65V to 1.95V	V_{CCB}=1.4V to 1.6V	V_{CCB}=1.1V to 1.3V	Units
	Min.	**Min.**	**Min.**	**Min.**	**Typ.**	
V_{CCA}=3.00V to 3.60V	140	120	100	80	40	Mbps
V_{CCA}=2.30V to 2.70V	120	120	100	80	40	Mbps
V_{CCA}=1.65V to 1.95V	100	100	80	60	40	Mbps
V_{CCA}=1.40V to 1.60V	80	80	60	60	40	Mbps
V_{CCA}=1.10V to 1.30V	**Typ.**	**Typ.**	**Typ.**	**Typ.**	**Typ.**	
	40	40	40	40	40	Mbps

Notes:

13. Maximum data rate is guaranteed, but not tested.
14. Maximum data rate is spec

I/O Architecture Benefit

The FXLA104 I/O architecture benefits the end user, beyond level translation, in the following three ways:

Auto Direction without an external direction pin.

Drive Capacitive Loads. Automatically shifts to a higher current drive mode only during “Dynamic Mode” or HL / LH transitions.

Lower Power Consumption. Automatically shifts to low-power mode during “Static Mode” (no transitions), lowering power consumption.

The FXLA104 does not require a direction pin. Instead, the I/O architecture detects input transitions on both side and automatically transfers the data to the corresponding output. For example, for a given channel, if both A and B side are at a static LOW, the direction has been established as A → B, and a LH transition occurs on the B port; the FXLA104 internal I/O architecture automatically changes direction from A → B to B → A.

During HL / LH transitions, or “Dynamic Mode,” a strong output driver drives the output channel in parallel with a weak output driver. After a typical delay of approximately 10ns – 50ns, the strong driver is turned off, leaving the weak driver enabled for holding the logic

Test Diagrams

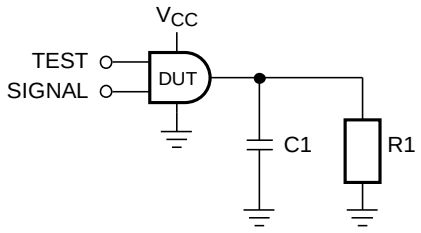


Figure 4. Test Circuit

Table 1. AC Test Conditions

Test	Input Signal	Output Enable Control
t_{PLH}, t_{PHL}	Data Pulses	0V
t_{PZL}	0V	HIGH to LOW Switch
t_{PZH}	V_{CCI}	HIGH to LOW Switch

Table 2. AC Load

V_{CCo}	C1	R1
1.2V±		

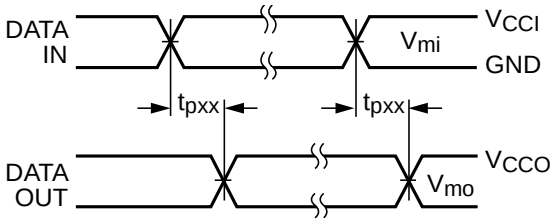


Figure 5. Waveform for Inverting and Non-Inverting Functions

Notes:

15. Input $t_R = t_F$ = 2.0ns, 10% to 90%.
16. Input $t_R = t_F$ = 2.5ns, 10% to 90%, at V_I = 3.0V to 3.6V only.

Figure 6. 3-State Output Low Enable Time for Low Voltage Logic

Notes:

17. Input $t_R = t_F$ = 2.0ns, 10% to 90%.
18. Input $t_R = t_F$ = 2.5ns, 10% to 90%, at V_I = 3.0V to 3.6V only.

Figure 7. 3-State Output High Enable Time for Low Voltage Logic

Notes:

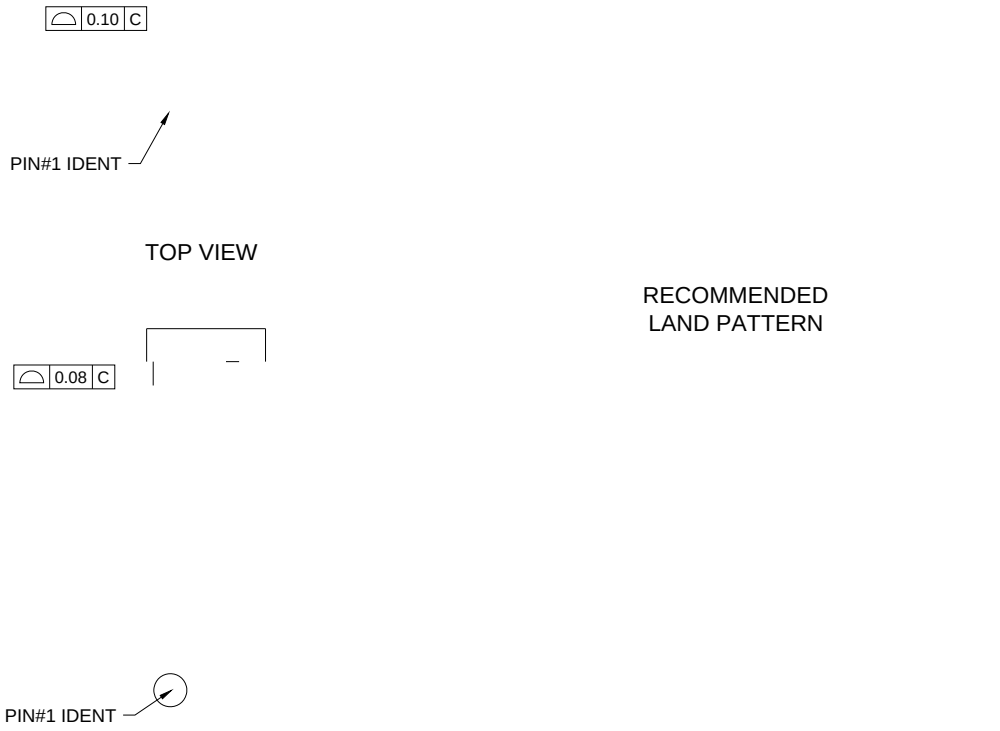
19. Input $t_R = t_F$ = 2.0ns, 10% to 90%.
20. Input $t_R = t_F$ = 2.5ns, 10% to 90%, at V_I = 3.0V to 3.6V only.

Table 3. Test Measure Points

Symbol

FXLA104 — Low-Voltage Dual-Supply 4-Bit Voltage Translator

Physical Dimensions



NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.
E. DRAWING FILENAME: MKT-UMLP16Arev4.
F. TERMINAL SHAPE MAY VARY ACCORDING TO PACKAGE SUPPLIER, SEE TERMINAL SHAPE VARIANTS.

Figure 12.16-Lead, UMLP, QUAD, Ultra-Thin MLP, 1.8 X 2.6mm

Physical Dimensions

RECOMMENDED
LAND PATTERN

DETAIL A
SCALE : 2X

NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.
E. DRAWING FILENAME: MKT-UMLP12Arev4.

LEAD
OPTION 1
SCALE : 2X

LEAD
OPTION 2
SCALE : 2X

Figure 13.12-Lead, UMLP, QUAD, JEDEC MO-252 1.8 x 1.8mm Package