			12-Lead, 1.7 mm x 2.0 mm Ultrathin Molded Leadless Package (UMLP)	5000 Units Tape and Reel

Pin Configuration

Figure 1. Top Through View

Pin Definitions

Pin #	Name	Description
1	V_{CCA}	A-Side Power Supply
2	A0	A-Side Inputs or 3-State Outputs
3	A1	A-Side Inputs or 3-State Outputs
4	A2	A-Side Inputs or 3-State Outputs
5	A3	A-Side Inputs or 3-State Outputs
6	GND	Ground
7		

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{CC}	Supply Voltage	V_{CCA}	-0.5	4.6	V
		V_{CCB}	-0.5	4.6	
V_I	DC Input Voltage	I/O Ports A and B	-0.5	4.6	V
		Control Input ($\overline{OE}$)	-0.5	4.6	
V_O	Output Voltage[2]	Output 3-State	-0.5	4.6	V
		Output Active (A_n)	-0.5	V_{CCA} +0.5	
		Output Active (B_n)	-0.5	V_{CCB} +0.5	
I_{IK}	DC Input Diode Current	V_{IN}<0V			

Power-Up/Power-Down Sequence

FXL translators offe33.7(e)-o80.5(oa)0.6(Sadv-56.5(lanu1.6(ans 0 10.4000002 59.2000008 739.1999754 cm /Im1 Do Q Be 739.1)9

AC Characteristics

V_{CCA} = 3.0 V to 3.6 V, T_A=-40 to 85°C

Symbol	Parameter	V_{CCB}=3.0 V to 3.6 V		V_{CCB}=2.3 V to 2.7 V		V_{CCB}=1.65 V to 1.95 V		V_{CCB}=1.4 V to 1.6 V		V_{CCB}=1.1 V to 1.3 V	Unit
		Min.	Max.	Min.	Max.	Min.	Max	Min.	Max.	Typ.	
t_{PLH},t_{PHL}	A to B	0.2	4.0	0.3	4.2	0.5	5.4	0.6	6.8	6.9	ns
	B to A	0.2	4.0	0.2	4.1	0.3	5.0	0.5	6.0	4.5	ns
t_{PZL},t_{PZH}	OE to A, OE to B		1.7		1.7		1.7		1.7	1.7	µs
t_{SKEW}	A Port, B Port (11)		0.5		0.5		0.5		1.0	1.0	ns

V_{CCA} = 2.3 V to 2.7 V, T_A=-40 to 85°C

Symbol	Parameter	V_{CCB}=3.0 V to 3.6 V		V_{CCB}=2.3 V to 2.7 V		V_{CCB}=1.65 V to 1.95 V		V_{CCB}=1.4 V to 1.6 V		V_{CCB}=1.1 V to 1.3 V	Unit
		Min.	Max.	Min.	Max.	Min.	Max	Min.	Max.	Typ.	
t_{PLH},t_{PHL}	A to B	0.2	4.1	0.4	4.5	0.5	5.6	0.8	6.9	7.0	ns
	B to A	0.3	4.2	0.4	4.5	0.5	5.5	0.5	6.5	4.8	ns
t_{PZL},t_{PZH}	OE to A, OE to B		1.7		1.7		1.7		1.7	1.7	µs
t_{SKEW}	A Port, B Port (11)		0.5		0.5		0.5		1.0	1.0	ns

V_{CCA} = 1.65 V to 1.95 V, T_A=-40 to 85°C

Symbol	Parameter	V_{CCB}=3.0 V to 3.6 V		V_{CCB}=2.3 V to 2.7 V		V_{CCB}=1.65 V to 1.95 V		V_{CCB}=1.4 V to 1.6 V		V_{CCB}=1.1 V to 1.3 V	Unit
		Min.	Max.	Min.	Max.	Min.	Max	Min.	Max.	Typ.	
t_{PLH},t_{PHL}	A to B	0.3	5.0	0.5	5.5	0.8	6.7	0.9	7.5	7.5	ns
	B to A	0.5	5.4	0.5	5.6	0.8	6.7	1.0	7.0	5.4	ns
t_{PZL},t_{PZH}	OE to A, OE to B		1.7		1.7		1.7		1.7	1.7	µs
t_{SKEW}	A Port, B Port (11)		0.5		0.5		0.5		1.0	1.0	ns

Note:

11. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (A_n or B_n) and switching with the same polarity (LOW-to-HIGH or HIGH-to-LOW) *(see Figure 10).* Skew is guaranteed, but not tested.

Maximum Data Rate[13, 14]

T_A=-40 to 85°C

V_{CCA}	V_{CCB}=3.0 V to 3.6 V	V_{CCB}=2.3V to 2.7V	V_{CCB}=1.65V to 1.95V	V_{CCB}=1.4V to 1.6V	V_{CCB}=1.1V to 1.3V	Unit
	Min.	Min.	Min.	Min.	Typ.	
V_{CCA}=3.00 to 3.60 V	140	120	100	80	40	Mbps
V_{CCA}=2.30 to 2.70 V	120	120	100	80	40	Mbps
V_{CCA}=1.65 to 1.95 V	100	100	80	60	40	Mbps
V_{CCA}=1.40 to 1.60 V	80	80	60	60	40	Mbps
V_{CCA}=1.10 to 1.30 V	Typ.	Typ.	Typ.	Typ.	Typ.	
	40	40	40	40	40	Mbps

Notes:

13. Maximum data rate is guaranteed, but not tested.
14. Maximum data rate is specified in megabits per second *(see Figure 9)*. It is equivalent to two times the).

I/O Architecture Benefit

The FXLA0104

Test Diagrams

Figure 3. Test Circuit

Table 1. AC Test Conditions

Test	Input Signal	Output Enable Control
t_{PLH}, t_{PHL}	Data Pulses	VCCA
t_{PZL}	0V	LOW to HIGH Switch
t_{PZH}	V_{CCI}	LOW to HIGH Switch

Table 2. AC Load

Figure 4. Waveform for Inverting and Non-Inverting Functions

Notes:

15. Input $t_R = t_F$ = 2.0 ns, 10% to 90%.
16. Input $t_R = t_F$ = 2.5 ns, 10% to 90%, at V_I = 3.0 V to 3.6 V only.