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FXL6408

Description

The FXL6408 is an 8−bit I²C−controlled GPIO expander. When configured in Input Mode, the FXL6408 monitors the input ports for data transitions and signals the baseband by asserting the $\overline{INT}$ pin. The input default values can be programmed independently, allowing customized input detection. All inputs can be configured with pull−up or pull−down resistors to pre−

PIN CONFIGURATION

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}, V_{DDIO}	Supply Voltages		−0.5	4.6	V
V_{IN}	DC Input Voltage		−0.5	4.0	V
V_{OUT}	Output Voltage (Note 1)		−0.5	4.0	V
I_{IK}	DC Input Diode Current	V_{IN} < 0 V		−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < 0 V		−50	mA
I_{OL}	DC Output Sink Current			+50	mA
I_{CC}	DC V_{CC} or Ground Current per Supply Pin			±100	mA
T_{STG}	Storage Temperature Range		−65	+150	°C
T_J	Junction Temperature under Bias			+150	°C
T_L	Junction Lead Temperature, Soldering 10 seconds			+260	°C
θ_{JA}	Thermal Resistance, Junction−to−Ambient			115	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22−A114		4	kV
		Charged Device Model, JESD22−C101		2	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All output current absolute maximum ratings must be observed.

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}	Supply Voltage Operating		1.65	3.60	V
V_{DDIO}	I/O Side Reference Voltage		1.65	4.00	V
V_{IN}	Input Voltage on I/O Pins		0	4.00	V
V_{OUT}	Output Voltage		0	V_{DDIO}	V
T_A	Operating Temperature		−40	+85	°C
t_r, t_f	Input Rise and Fall Times to I/O Pins when Configured as Inputs	V_{DDIO} at 1.8 V, 2.5 V ±0.2 V	0	200	ns/V

Table 4. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			T_A = −40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
RST, ADDR, SDA, SCL, $\overline{INT}$ Pins									
V_{POR}	Power−On Reset Voltage	V_{DDIO} = 0 to 4.0 V				1.25		1.25	V
I_{IN}	Input Leakage Current	$0 \le V_{IN} \le V_{CCCC0}$							

Table 5. AC ELECTRICAL CHARACTERISTICS (All typical values are for V_{CC} = 1.8 V at T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Fast Mode		Unit
		Min	Max	
t_W	Reset Pulse Duration (see Figure 3)	150		ns
t_{RST_GLITCH}	Input Glitch Rejection on RST Pin (see Figure 3)	50	150	ns
t_{RESET}	Reset Time, Total Time from Rising Edge of Reset Pulse to Falling Edge of $\overline{INT}$ Pin (see Figure 4)		150	ns
t_{IV}	Time from Input Default State Change to $\overline{INT}$ Pin Driven LOW (see Figure 5)		4	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 6. DC CHARACTERISTICS (I^2C CONTROLLER SDA, SCL)

DEFINITION OF TIMING

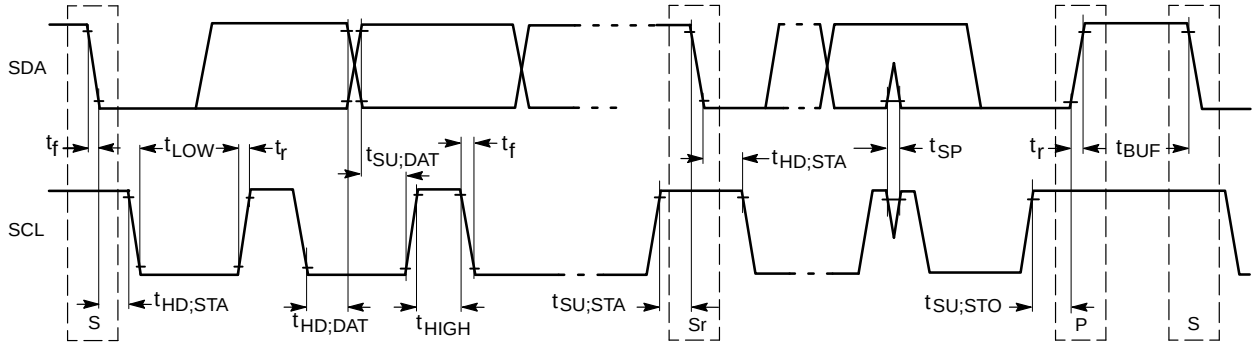

Figure 6. Definition of Timing for Full−Speed Mode Devices on the I²C Bus

FUNCTIONAL DESCRIPTION

Overview

The FXL6408 I/O expander frees up six ports of the central processor to be dedicated for more critical functions. The FXL6408 enables the addition of eight General−Purpose Input / Output (GPIO) ports to a system processor while using two I/O ports for I^2C control (net six additional I/Os). The device can be used in multiple applications, from button monitoring to driving control pins of other ICs in the system. It also allows the system designer to add new features and functions quickly without upgrading the central processor. The FXL6408 includes eight I/O pins controlled by an integrated I^2C slave and allows the central processor to control each I/O independently. When configured as outputs, each pin can deliver up to 6 mA drive. When configured as inputs, the default state can be independently configured. In addition, the FXL6408 has integrated pull−up and pull−down resistors that are enabled via I^2C commands in the register map. This allows the system designer to pre−bias the inputs to a known level to allow use with un−driven input signals.

Interrupt Operation

The $\overline{INT}$ pin is a LOW−asserted open−drain output and requires an external pull−up resistor. The FXL6408 signals an interrupt to the processor when an event occurs, removing the need for the processor to continuously poll the FXL6408 registers. Immediately after detecting a change at an input, the FXL6408 writes the corresponding bit in the input interrupt status register (13_h) and asserts the $\overline{INT}$ pin by pulling it LOW. The interrupt status register bit remains HIGH until the processor reads the register and clears the bit. If the input pin remains in the non−default state after the interrupt has been serviced, a new interrupt is not generated until after the input state has first returned to its default state and changed back to its non−default state. The FXL6408 also contains an Input Status register ($0F_h$) used to verify the current status of the given input at the time when the interrupt is serviced by the processor. These two registers allow the processor to determine the following information

Translation

The FXL6408 has the ability to translate between the

Table 9. I

Table 12. OUTPUT STATE (Address 05_h; if the pin is defined as input in register 03_h, the corresponding bit has no effect)

Bit #	Name	Bit Size	Description
7	Out 7	1	0: GPIO Output = LOW 1: GPIO Output = HIGH
6	Out 6	1	
5	Out 5	1	
4	Out 4	1	
3	Out 3	1	
2	Out 2	1	
1	Out 1	1	
0	Out 0	1	

Table 13. OUTPUT HIGH−Z (Address 07_h; if the pin is defined as input in register 03_h, the corresponding bit has no effect)

Bit #	Name	Bit Size	Description
7	Out 7	1	0: GPIO Output state follows register 05_h 1: GPIO Output = HIGH−Z
6	Out 6	1	
5	Out 5	1	
4	Out 4	1	
3	Out 3	1	
2	Out 2	1	
1	Out 1	1	
0			

Table 15. PULL ENABLE (Address 0B

Table 18. INTERRUPT MASK (Address 11_h; if the pin is defined as output in register 03_h, the corresponding bit has no effect; this bit enables the interrupt generation from input pin state change to INT)

Bit #	Name	Bit Size	Desce80 Tc(ea58l1(56.5754208.743 694.998 .9071 15.351 3189

UQFN16 1.80x2.60x0.50, 0.40P
CASE 523BF
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DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.45	0.50	0.5

SIDE VIEW

BOTTOM VIEW