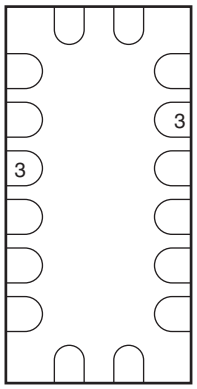
Is Now Part of

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

Connection Diagrams



DQFN Pad Assignments (Top Through View)

MicroMLP Pad Assignments (Top Through View)

Top Mark

MicroMLP Top Mark (Top View)

Pin Assignment

DQFN Pin #	µMLP Pin #	Terminal Name	Description
1	3	V_{CCA}	Side A Power Supply
2	4	$T/\overline{R}_0$	Transmit/Receive Input
3–6	5–8	A_0–A_3	Side A Inputs or 3-STATE Outputs
7	9	$T/\overline{R}_3$	Transmit/Receive Input
8	10	GND	Ground
9	11	$\overline{OE}$	Output Enable Input
10	12	$T/\overline{R}_2$	Transmit/Receive Input
11–14	13–16	B_3–B_0	Side B Inputs or 3-STATE Outputs
15	1	$T/\overline{R}_1$	Transmit/Receive Input
16	2	V_{CCB}	Side B Power Supply

Truth Table

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Power-Up/Power-Down Sequencing

FXL translators offer an advantage in that either V_{CC} may be powered up first. This benefit derives from the chip design. When either V_{CC} is at 0 volts, outputs are in a HIGH-Impedance state. The control inputs ($T/\overline{R}_n$ and $\overline{OE}$) are designed to track the V_{CCA} supply. A pull-up resistor tying $\overline{OE}$ to V_{CCA} should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power-up/power-down. The size of the pull-up resistor is based upon the current-sinking capability of the $\overline{OE}$ driver.

The recommended power-up sequence is the following:

1. Apply power to either V_{CC}.
2. Apply power to the $T/\overline{R}_n$ inputs (Logic HIGH for A-to-B operation; Logic LOW for B-to-A operation) and to the respective data inputs (A Port or B Port). This may occur at the same time as Step 1.
3. Apply power to other V_{CC}.
4. Drive the $\overline{OE}$ input LOW to enable the device.

The recommended power-down sequence is the following:

1. Drive $\overline{OE}$ input HIGH to disable the device.
2. Remove power from either V_{CC}.
3. Remove power from other V_{CC}.

Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions(2)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Notes:

1. I_O Absolute Maximum Rating must be observed.
2. All unused inputs and I/O pins must be held at V_{CCI}

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CCI} (V)	V_{CCO} (V)	Min.	Max.	Units
V_{IH}	High Level Input Voltage[3]	Data Inputs A_n, B_n	2.7–3.6	1.1–3.6	2.0		V
			2.3–2.7		1.6		
			1.65–2.3		0.65 x V_{CCI}		
			1.4–1.65		0.65 x V_{CCI}		
			1.1–1.4		0.9 x V_{CCI}		

I_I	Input Leakage Current. Control Pins	$V_I = V_{CCA}$ or GND	1.1–3.6	3.6	±1.0	µA
I_{OFF}	Power Off Leakage Current	A_n, V_I or V_O = 0V to 3.6V	0	3.6	±10.0	µA
		B_n, V_I or V_O = 0V to 3.6V	3.6	0	±10.0	
I_{OZ}	3-STATE Output Leakage[5] $0 \le V_O \le 3.6V$ $V_I = V_{IH}$ or V_{IL}	A_n, B_n $\overline{OE} = V_{IH}$	3.6	3.6	±10.0	µA
		B_n, $\overline{OE}$ = Don't Care	0	3.6	+10.0	
		A_n, $\overline{OE}$ = Don't Care	3.6	0	+10.0	
$I_{CCA/B}$	Quiescent Supply Current[6]	$V_I = V_{CCI}$ or GND; $I_O = 0$	1.1–3.6	1.1–3.6	20.0	µA
I_{CCZ}	Quiescent Supply Current[6]	V_I				

Notes:

3. V_{CCI} = the V_{CC} associated with the data input under test.
4. V_{CCO} = the V_{CC} associated with the output under test.
5. Don't Care = Any valid logic level.
6. Reflects current per supply, V_{CCA} or V_{CCB}.

Reel Dimensions inches (millimeters)

Tape Size	A	B	C	D	N	W1	W2
12 mm	13.0 (330)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	7.008 (178)	0.488 (12.4)	0.724 (18.4)

Physical Dimensions

Figure 5. 16-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241 2.5 x 3.5mm

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner

[redacted]